

## 1Gb LPDDR3 Specification

### Specifications

- **Density:** 1G bits
- **Organization**
  - 4 banks x 8M x 32 bits
- **Power Supply**
  - VDD1=1.7 to 1.95V
  - VDD2 ,VDDQ=1.14 to 1.3V
- **Clock Frequency(MHz)**
  - 933(\*)/800/667/533MHz
  - (max.) (\* : with VDD2, VDDQ=1.17V to 1.3V)
- **Page Size :** 4KB
  - Row address: AX0 to AX12
  - Column address: AY0 to AY9
- **x32:** 4 internal banks for concurrent operation
- **Interface:** HSUL\_12
- **Burst lengths (BL):** 8
- **Read latency (RL):** 3, 6, 8, 9, 10, 11, 12, 14, 16
- **Write latency (WL):** 1, 3, 4, 5, 6, 8, 9, 11, 13
- **Precharge:** auto precharge option for each burst access
- **Programmable Driver Strength**
- **Refresh:** auto-refresh, self-refresh
- **Average Refresh Period:**
  - 7.8uS @ <85°C
  - 1.95uS @ <105°C
- **Operating Temperature range**
  - T<sub>OPER</sub> = -25°C to +85°C
  - T<sub>OPER</sub> = -40°C to +105°C (extended range)

### Features

- DLL is not implemented
- Low power consumption
- JEDEC LPDDR3-compliance
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 8n prefetch pipelined architecture
- Differential clock inputs (CK\_t and CK\_c)
- Commands entered on each positive CK\_t edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data

### **Differences from JEDEC:**

This 1Gb LPDDR3 device is not part of JEDEC JESD209-3B specification. It follows JEDEC specification except for the reduction in address space which is also reflected in Mode Register 8, Mode Register 9 bit [5] is a readable Failed Die Bit. VDD2,VDDQ=1.17 to 1.3V if need use 933MHz.

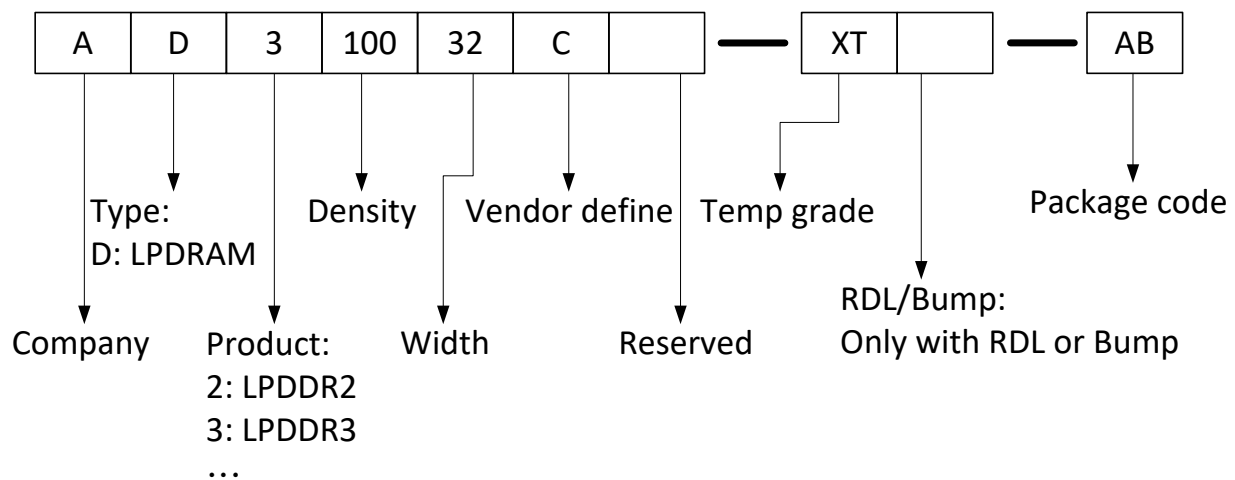
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## 1 Ordering Information:

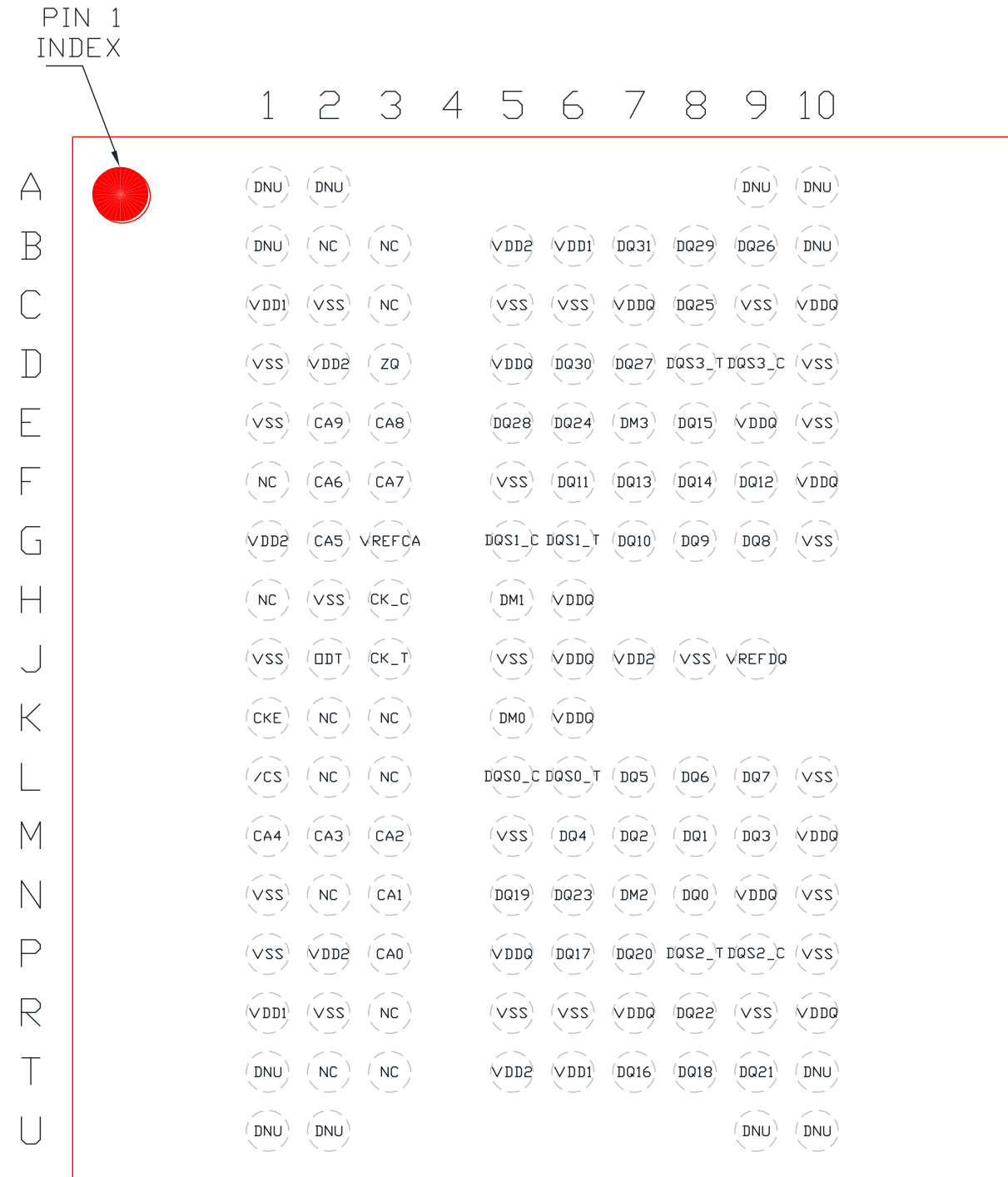
Die Part Number	Configuration	Temperature Range	Max Frequency	Note
AD310032C	X32	-25°C to +85°C	933 MHz	KGD
AD310032C-X	X32	-40°C to +85°C	933 MHz	KGD
AD310032C-XT	X32	-40°C to +105°C	933 MHz	KGD
AD310032C-AB	X32	-25°C to +85°C	933 MHz	PKG 134B (10x11.5) (only for validation purpose)

## IOT\_LPDDR\_PN rule



## 2 Package Ball Assignment

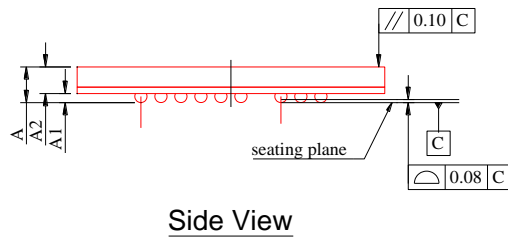
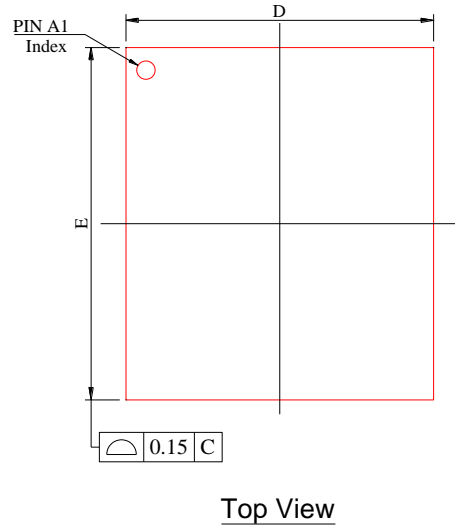
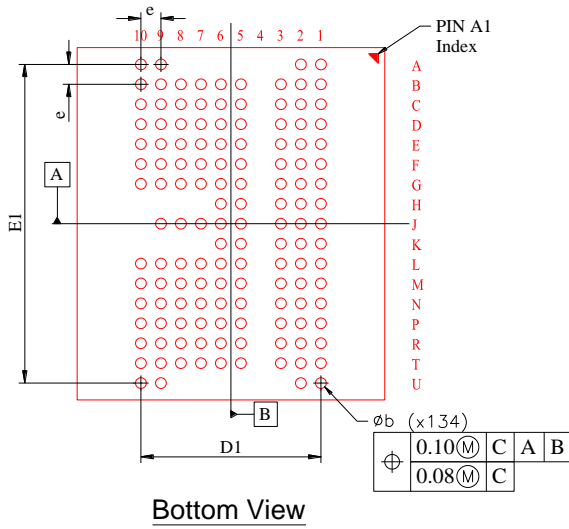
x32: "134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)"



# Top View Through Package

### 3 Package Outline Drawing

x32: “134-Ball FBGA –10x11.5x1.0 mm, ball pitch 0.65 mm, ball size 0.4 mm. (package code AB)”



Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.27	0.32	0.37
A2	0.545	0.58	0.63
D	9.90	10.00	10.10
D1	5.85 BSC		
E	11.40	11.50	11.60
E1	10.40 BSC		
b	0.35	0.40	0.45
e	0.65 BSC		

## 4 Electrical Specifications:

All voltages are referenced to each GND level ( $V_{SS}$  and  $V_{SSQ}$ ).

Execute power-up and Initialization sequence before proper device operation can be achieved.

### 4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.4 to +1.6	V	
Power supply voltage (core power1) relative to $V_{SS}$	$V_{DD1}$	-0.4 to +2.3	V	
Power supply voltage (core power2) relative to $V_{SS}$	$V_{DD2}$	-0.4 to +1.6	V	
Power supply voltage for output relative to $V_{SSQ}$	$V_{DDQ}$	-0.4 to +1.6	V	
Storage temperature	$T_{STG}$	-55 to +125	°C	1
Power dissipation	PD	1.0	W	

Notes:

- Storage temperature the case surface temperature on the center/top side of the DRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 4.2 Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Standard	$T_{OPER}$	-25 to +85	°C	1
Extended		-40 to +105	°C	1

Notes:

- Operating temperature refers to  $T_j$  of DRAM

#### 4.3 Recommended DC Operating Conditions

( $T_{\text{OPER}} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ )

Parameter		Symbol	min.	typical	max	Unit	Notes
Supply voltage	Core Power1	$V_{\text{DD1}}$	1.7	1.8	1.95	V	1
		$V_{\text{SS}}$	0	0	0	V	
	Core Power2	$V_{\text{DD2}}$	1.14	1.2	1.3	V	1
		$V_{\text{SS}}$	0	0	0	V	
	I/O Buffer Power	$V_{\text{DDQ}}$	1.14	1.2	1.3	V	1
		$V_{\text{SSQ}}$	0	0	0	V	

Notes:

- $V_{\text{DDQ}}$  tracks with  $V_{\text{DD2}}$ . AC parameters are measured with  $V_{\text{DD2}}$  and  $V_{\text{DDQ}}$  tied together.

#### 4.4 AC and DC Input Measurement Levels

[Refer to section 7 in JEDEC Standard No. 209-3B]

#### 4.5 AC and DC Output Measurement Levels

[Refer to section 8 in JEDEC Standard No. 209-3B]



**4.6 DC Characteristics 1**
 $(T_{OPER} = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{DD1} = 1.7\text{V to } 1.95\text{V}, V_{DD2}/V_{DDQ} = 1.14\text{V to } 1.3\text{V}, V_{SS}/V_{SSQ} = 0\text{V})$ 

Parameter	Test Condition	Symbol	Power Supply	Max (x32)				Unit
				DDR 1866	DDR 1600	DDR 1333	DDR 1066	
Operating one bank active-precharge current	$t_{CK} = t_{CK(min)}$ ; $t_{RC} = t_{RC(min)}$ ; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD01</sub>	V <sub>DD1</sub>	27				mA
		I <sub>DD02</sub>	V <sub>DD2</sub>	120				mA
		I <sub>DD0IN</sub>	V <sub>DDQ</sub>	1				mA
Idle power-down standby current	$t_{CK} = t_{CK(min)}$ ; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD2P1</sub>	V <sub>DD1</sub>	0.8				mA
		I <sub>DD2P2</sub>	V <sub>DD2</sub>	1.4				mA
		I <sub>DD2PIN</sub>	V <sub>DDQ</sub>	1				mA
Idle power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE;	I <sub>DD2PS1</sub>	V <sub>DD1</sub>	0.8				mA
		I <sub>DD2PS2</sub>	V <sub>DD2</sub>	1.4				mA
		I <sub>DD2PSIN</sub>	V <sub>DDQ</sub>	1				mA
Idle non power-down standby current	$t_{CK} = t_{CK(min)}$ ; CKE is HIGH; CS_n is HIGH; all banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD2N1</sub>	V <sub>DD1</sub>	0.8				mA
		I <sub>DD2N2</sub>	V <sub>DD2</sub>	35				mA
		I <sub>DD2NIN</sub>	V <sub>DDQ</sub>	1				mA
Idle non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; all banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE	I <sub>DD2NS1</sub>	V <sub>DD1</sub>	0.8				mA
		I <sub>DD2NS2</sub>	V <sub>DD2</sub>	18				mA
		I <sub>DD2NSIN</sub>	V <sub>DDQ</sub>	1				mA
Active power-down standby current	$t_{CK} = t_{CK(min)}$ ; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD3P1</sub>	V <sub>DD1</sub>	1.5				mA
		I <sub>DD3P2</sub>	V <sub>DD2</sub>	10				mA
		I <sub>DD3PIN</sub>	V <sub>DDQ</sub>	1				mA
Active power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is LOW; CS_n is HIGH; one bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	I <sub>DD3PS1</sub>	V <sub>DD1</sub>	1.5				mA
		I <sub>DD3PS2</sub>	V <sub>DD2</sub>	10				mA
		I <sub>DD3PSIN</sub>	V <sub>DDQ</sub>	1				mA
Active non power-down standby current	$t_{CK} = t_{CK(min)}$ ; CKE is HIGH; CS_n is HIGH; one bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD3N1</sub>	V <sub>DD1</sub>	1.5				mA
		I <sub>DD3N2</sub>	V <sub>DD2</sub>	42				mA
		I <sub>DD3NIN</sub>	V <sub>DDQ</sub>	1				mA
Active non power-down standby current with clock stop	CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE	I <sub>DD3NS1</sub>	V <sub>DD1</sub>	1.5				mA
		I <sub>DD3NS2</sub>	V <sub>DD2</sub>	26				mA
		I <sub>DD3NSIN</sub>	V <sub>DDQ</sub>	1				mA

Parameter	Test Condition	Symbol	Power Supply	Max (x32)				Unit
				DDR 1866	DDR 1600	DDR 1333	DDR 1066	
Operating burst read current	$t_{CK} = t_{CK(min)}$ ; CS_n is HIGH between valid commands; one bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	I <sub>DD4R1</sub>	V <sub>DD1</sub>	39	33	27	22	mA
		I <sub>DD4R2</sub>	V <sub>DD2</sub>	265	235	205	170	mA
Operating burst write current	$t_{CK} = t_{CK(min)}$ ; CS_n is HIGH between valid commands; one bank active; BL = 4; WL = WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	I <sub>DD4W1</sub>	V <sub>DD1</sub>	39	33	27	22	mA
		I <sub>DD4W2</sub>	V <sub>DD2</sub>	315	280	240	205	mA
		I <sub>DD4WIN</sub>	V <sub>DDQ</sub>	40				mA
All Bank Auto Refresh Burst Current	$t_{CK} = t_{CK(min)}$ ; CS_n is HIGH between valid commands; $t_{RC} = t_{RFCab(min)}$ ; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD51</sub>	V <sub>DD1</sub>	40				mA
		I <sub>DD52</sub>	V <sub>DD2</sub>	160				mA
		I <sub>DD5IN</sub>	V <sub>DDQ</sub>	1				mA
All Bank Auto Refresh Average Current	$t_{CK} = t_{CK(min)}$ ; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$ ; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD5ab1</sub>	V <sub>DD1</sub>	2				mA
		I <sub>DD5ab2</sub>	V <sub>DD2</sub>	40				mA
		I <sub>DD5abIN</sub>	V <sub>DDQ</sub>	1				mA
Per Bank Auto Refresh Average Current	$t_{CK} = t_{CK(min)}$ ; CKE is HIGH between valid commands; $t_{RC} = t_{REFI/8}$ ; CA bus inputs are SWITCHING; Data bus inputs are STABLE	I <sub>DD5pb1</sub>	V <sub>DD1</sub>	2				mA
		I <sub>DD5pb2</sub>	V <sub>DD2</sub>	40				mA
		I <sub>DD5pbIN</sub>	V <sub>DDQ</sub>	1				mA
Self Refresh Current (Standard Temperature Range: -40°C to 85°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 1x Self-refresh rate	I <sub>DD61</sub>	V <sub>DD1</sub>	1				mA
		I <sub>DD62</sub>	V <sub>DD2</sub>	2				mA
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	0.3				mA
Deep Power Down Current (Standard Temperature Range: -40°C to 85°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	I <sub>DD81</sub>	V <sub>DD1</sub>	0.2				mA
		I <sub>DD82</sub>	V <sub>DD2</sub>	0.6				mA
		I <sub>DD8IN</sub>	V <sub>DDQ</sub>	0.3				mA
Self Refresh Current (Extended Temperature Range: 85°C to 105°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE; Maximum 4x Self-refresh rate	I <sub>DD6ET1</sub>	V <sub>DD1</sub>	2				mA
		I <sub>DD6ET2</sub>	V <sub>DD2</sub>	4				mA
		I <sub>DD6ETIN</sub>	V <sub>DDQ</sub>	1				mA
Deep Power Down Current (Extended Temperature Range: 85°C to 105°C)	CK_t = LOW; CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	I <sub>DD8ET1</sub>	V <sub>DD1</sub>	0.4				mA
		I <sub>DD8ET2</sub>	V <sub>DD2</sub>	1				mA
		I <sub>DD8ETIN</sub>	V <sub>DDQ</sub>	1				mA

**4.7 Advanced Data Retention Current (Self-refresh current)**

 ( $T_{\text{OPER}} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{\text{DD1}} = 1.7\text{V}$  to  $1.95\text{V}$ ,  $V_{\text{DD2}}/V_{\text{DDQ}} = 1.14\text{V}$  to  $1.3\text{V}$ ,  $V_{\text{SS}}/V_{\text{SSQ}} = 0\text{V}$ )

Parameter	Symbol	supply	Typical	Unit	Test Condition	
+25°C CKE ≤ 0.2V	Full Array	$I_{\text{DD61}}$	$V_{\text{DD1}}$	88	μA	All devices are in self-refresh CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		$I_{\text{DD62}}$	$V_{\text{DD2}}$	180	μA	
		$I_{\text{DD6IN}}$	$V_{\text{DDQ}}$	6	μA	
	1/2 Array	$I_{\text{DD61}}$	$V_{\text{DD1}}$	76	μA	
		$I_{\text{DD62}}$	$V_{\text{DD2}}$	133	μA	
		$I_{\text{DD6IN}}$	$V_{\text{DDQ}}$	6	μA	
	1/4 Array	$I_{\text{DD61}}$	$V_{\text{DD1}}$	65	μA	
		$I_{\text{DD62}}$	$V_{\text{DD2}}$	95	μA	
		$I_{\text{DD6IN}}$	$V_{\text{DDQ}}$	6	μA	
	1/8 Array	$I_{\text{DD61}}$	$V_{\text{DD1}}$	59	μA	
		$I_{\text{DD62}}$	$V_{\text{DD2}}$	74	μA	
		$I_{\text{DD6IN}}$	$V_{\text{DDQ}}$	6	μA	

Parameter	Symbol	supply	max	Unit	Test Condition	
$+45^{\circ}\text{C} \leq T_{\text{OPER}} \leq +85^{\circ}\text{C}$ CKE $\leq 0.2\text{V}$	Full Array	I <sub>DD61</sub>	V <sub>DD1</sub>	1	mA	All devices are in self-refresh CK <sub>t</sub> = LOW, CK <sub>c</sub> = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE
		I <sub>DD62</sub>	V <sub>DD2</sub>	1.6	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	0.3	mA	
	1/2 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	0.8	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	1.2	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	0.3	mA	
	1/4 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	0.7	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	1	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	0.3	mA	
	1/8 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	0.65	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	0.9	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	0.3	mA	
$+85^{\circ}\text{C} \leq T_{\text{OPER}} \leq +105^{\circ}\text{C}$ CKE $\leq 0.2\text{V}$	Full Array	I <sub>DD61</sub>	V <sub>DD1</sub>	2	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	4	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	1	mA	
	1/2 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	1.6	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	2.7	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	1	mA	
	1/4 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	1.4	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	1.7	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	1	mA	
	1/8 Array	I <sub>DD61</sub>	V <sub>DD1</sub>	1.3	mA	
		I <sub>DD62</sub>	V <sub>DD2</sub>	1.4	mA	
		I <sub>DD6IN</sub>	V <sub>DDQ</sub>	1	mA	

**Notes:**

This device supports bank-masking.

I<sub>DD6</sub> 85°C is the maximum and I<sub>DD6</sub> 25°C typical of the distribution of the arithmetic mean.

#### 4.8 DC Characteristics 2

( $T_{OPER} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{DD1} = 1.7\text{V}$  to  $1.95\text{V}$ ,  $V_{DD2}/V_{DDQ} = 1.14\text{V}$  to  $1.3\text{V}$ ,  $V_{SS}/V_{SSQ} = 0\text{V}$ )

Parameter	Symbol	min.	max	Unit	Test Condition	Notes
Input leakage current	$I_{LI}$	-5.0	5.0	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{DDQ}$	
Output leakage current	$I_{LO}$	-20	20	$\mu\text{A}$	$0 \leq V_{OUT} \leq V_{DDQ}$ DQ/DQS/DQSB = disabled	
Output high voltage	$V_{OH}$	$0.9 \times V_{DDQ}$	--	V	$I_{OH} = -0.1\text{mA}$	
Output low voltage	$V_{OL}$	--	$0.1 \times V_{DDQ}$	V	$I_{OL} = 0.1\text{mA}$ ODT = disabled	
Output low voltage (ODT)	$V_{OL}$	--	$V_{DDQ} \times [0.1 + 0.9 \times (R_{ON} / (R_{TT} + R_{ON}))]$	V	$I_{OL} = 0.1\text{mA}$ ODT = enabled	1

Notes:

- The min value is derived when using  $R_{TT,min}$  and  $R_{ON,max}$  ( $\pm 30\%$  uncalibrated,  $\pm 15\%$  calibrated).

#### 4.9 Differential Input Cross Point Voltage

( $T_{OPER} = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{DD1} = 1.7\text{V}$  to  $1.95\text{V}$ ,  $V_{DD2}/V_{DDQ} = 1.14\text{V}$  to  $1.3\text{V}$ ,  $V_{SS}/V_{SSQ} = 0\text{V}$ )

Parameter	Symbol	min.	max	Unit	Notes
Differential Input Cross Point Voltage relative to $V_{DD2}/2$ for CK_t, CK_c	$V_{IXCA}$	-120	120	mV	1,2
Differential Input Cross Point Voltage relative to $V_{DDQ}/2$ for DQS_t, DQS_c	$V_{IXDQ}$	-120	120	mV	1,2

Notes:

- The typical value of  $V_{IX(AC)}$  is expected to be about  $0.5 \times V_{DD}$  of the transmitting device, and  $V_{IX(AC)}$  is expected to track variations in  $V_{DD}$ .  $V_{IX(AC)}$  indicates the voltage at which differential input signals must cross.
- For CK\_t and CK\_c,  $V_{Ref} = V_{RecCA(DC)}$ . For DQS\_t and DQS\_c,  $V_{Ref} = V_{RefDQ(DC)}$ .

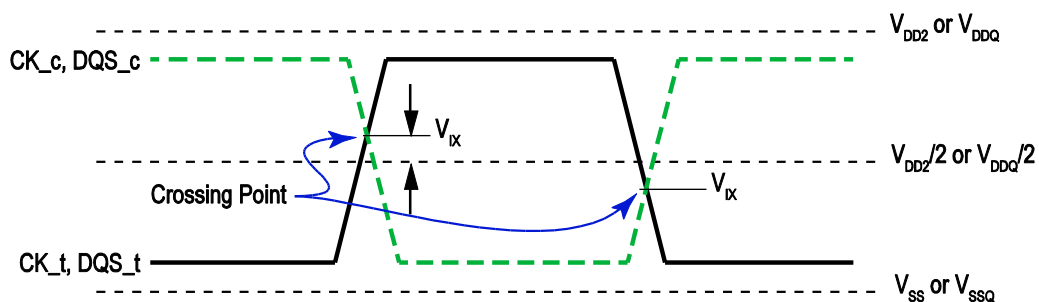


Figure 1. Differential Signal Levels

#### 4.10 Pin Capacitance

( $T_{OPER} = +25^{\circ}C$ ,  $V_{DD1} = 1.7V$  to  $1.95V$ ,  $V_{DD2}/V_{DDQ} = 1.14V$  to  $1.3V$ ,  $V_{SS}/V_{SSQ} = 0V$ )

Parameter	Symbol		LPDDR3	Unit	Notes
CLK input pin capacitance CK_t, CK_c	$C_{CK}$	min.	0.5	pF	1,2
		max	1.2		
CLK input pin capacitance $\Delta$ CK_t, CK_c	$C_{DCK}$	min.	0	pF	1,2,3
		max	0.15		
Input pin capacitance CA, CS_n, CKE	$C_I$	min.	0.5	pF	1,2,4
		max	1.1		
Input pin capacitance $\Delta$ CA, CS_n, CKE	$C_{DI}$	min.	-0.2	pF	1,2,5
		max	0.2		
Input/output pin capacitance DQS_t, DQS_c, DQ, DM	$C_{IO}$	min.	1.0	pF	1,2,6,7
		max	1.8		
Input/output pin capacitance $\Delta$ DQS_t, DQS_c	$C_{DDQS}$	min.	0	pF	1,2,7,8
		max	0.2		
Input/output pin capacitance $\Delta$ DQ, DM	$C_{DIO}$	min.	-0.25	pF	1,2,7,9
		max	0.25		
Calibration pin capacitance	$C_{2Q}$	min.	0	pF	1,2
		max	2.0		

Notes:

1. This parameter applies to die device only (does not include package capacitance)
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with  $V_{DD1}$ ,  $V_{DD2}$ ,  $V_{DDQ}$ ,  $V_{SS}$ ,  $V_{SSQ}$  applied and all other pins floating.
3. Absolute value of  $C_{CK\_t}-C_{CK\_c}$ .
4.  $C_I$  applies to CS\_n, CKE, CA0-CA9, ODT.
5.  $C_{DI}=C_I-0.5 \times (C_{CK\_t}+C_{CK\_c})$
6. DM loading matches DQ and DQS
7. MR3 I/O configuration DS OP3-OP0=4'b0001 (34.3 $\Omega$  typical)
8. Absolute value of  $C_{DQS\_t}$  and  $C_{DQS\_c}$ .
9.  $C_{DIO}=C_{IO}-0.5 \times (C_{DQS\_t}+C_{DQS\_c})$  in byte-lane.

#### 4.11 Refresh Requirement Parameters (1GB x32)

Parameter	Symbol	Value	Unit
Number of Banks		4	
Refresh Window $T_{CASE} \leq 85^{\circ}C$	$t_{REFW}$	32	ms
Required number of REFRESH commands (min)	R	4,096	
Average time between REFRESH commands $T_{CASE} \leq 85^{\circ}C$	$t_{REFI}$	7.8	$\mu s$
All Bank Refresh Cycle time	$t_{RFCab}$	130	ns
Per Bank Refresh Cycle time	$t_{RFCpb}$	60	ns

**4.12 AC Characteristics**

 (T<sub>OPER</sub> = -40°C to +105°C, V<sub>DD1</sub> = 1.7V to 1.95V, V<sub>DD2</sub>/V<sub>DDQ</sub> = 1.14V to 1.3V, V<sub>SS</sub>/V<sub>SSQ</sub> = 0V)

Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	
Max. Frequency		~	933	800	733	667	600	533	400	MHz
Clock Timing										
Average Clock Period	t <sub>CK</sub> (avg)	min	1.071	1.25	1.364	1.5	1.667	1.875	2.5	ns
		max	100							
Average high pulse width	t <sub>CH</sub> (avg)	min	0.45							t <sub>CK</sub> (avg)
		max	0.55							
Average low pulse width	t <sub>CL</sub> (avg)	min	0.45							t <sub>CK</sub> (avg)
		max	0.55							
Absolute Clock Period	t <sub>CK</sub> (abs)	min	t <sub>CK</sub> (avg)(min) + t <sub>JIT</sub> (per)(min)							ns
Absolute clock HIGH pulse width (with allowed jitter)	t <sub>CH</sub> (abs)	min	0.43							t <sub>CK</sub> (avg)
		max	0.57							
Absolute clock LOW pulse width (with allowed jitter)	t <sub>CL</sub> (abs)	min	0.43							t <sub>CK</sub> (avg)
		max	0.57							
Clock Period Jitter (with allowed jitter)	t <sub>JIT</sub> (per)	min	-60	-70	-75	-80	-85	-90	-100	ps
		max	60	70	75	80	85	90	100	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	t <sub>JIT</sub> (cc)	max	120	140	150	160	170	180	200	ps
Duty cycle Jitter (with allowed jitter)	t <sub>JIT</sub> (duty) allowed	min	min((t <sub>CH</sub> (abs), min - t <sub>CH</sub> (avg), min) (t <sub>CL</sub> (abs), min - t <sub>CL</sub> (avg), min)) x t <sub>CK</sub> (avg)							ps
		max	max((t <sub>CH</sub> (abs), max - t <sub>CH</sub> (avg), max) (t <sub>CL</sub> (abs), max - t <sub>CL</sub> (avg), max)) x t <sub>CK</sub> (avg)							
Cumulative error across 2 cycles	t <sub>ERR</sub> (2per) allowed	min	-88	-103	-111	-118	-125	-132	-147	ps
		max	88	103	111	118	125	132	147	
Cumulative error across 3 cycles	t <sub>ERR</sub> (3per) allowed	min	-105	-122	-131	-140	-149	-157	-175	ps
		max	105	122	131	140	149	157	175	
Cumulative error across 4 cycles	t <sub>ERR</sub> (4per) allowed	min	-117	-136	-146	-155	-165	-175	-194	ps
		max	117	136	146	155	165	175	194	
Cumulative error across 5 cycles	t <sub>ERR</sub> (5per) allowed	min	-126	-147	-158	-168	-178	-188	-209	ps
		max	126	147	158	168	178	188	209	
Cumulative error across 6 cycles	t <sub>ERR</sub> (6per) allowed	min	-133	-155	-166	-177	-189	-200	-222	ps
		max	133	155	166	177	189	200	222	
Cumulative error across 7 cycles	t <sub>ERR</sub> (7per) allowed	min	-139	-163	-175	-186	-198	-209	-232	ps
		max	139	163	175	186	198	209	232	
Cumulative error across 8 cycles	t <sub>ERR</sub> (8per) allowed	min	-145	-169	-181	-193	-205	-217	-241	ps
		max	145	169	181	193	205	217	241	

Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	MT/s
Max. Frequency		~	933	800	733	667	600	533	400	MHz
Clock Timing										
Cumulative error across 9 cycles	$t_{ERR(9per)}$ allowed	min	-150	-175	-188	-200	-212	-224	-249	ps
		max	150	175	188	200	212	224	249	
Cumulative error across 10 cycles	$t_{ERR(10per)}$ allowed	min	-154	-180	-193	-205	-218	-231	-257	ps
		max	154	180	193	205	218	231	257	
Cumulative error across 11 cycles	$t_{ERR(11per)}$ allowed	min	-158	-184	-197	-210	-224	-237	-263	ps
		max	158	184	197	210	224	237	263	
Cumulative error across 12 cycles	$t_{ERR(12per)}$ allowed	min	-161	-188	-202	-215	-229	-242	-269	ps
		max	161	188	202	215	229	242	269	
Cumulative error across n = 13, 14 ... 49, 50 cycles	$t_{ERR(nper)}$ allowed	min	$t_{ERR(nper)}$ , allowed, min = $(1 + 0.68\ln(n)) \times t_{JIT(per)}$ , allowed, min							ps
		max	$t_{ERR(nper)}$ , allowed, max = $(1 + 0.68\ln(n)) \times t_{JIT(per)}$ , allowed, max							
ZQ Calibration Parameters										
Initialization Calibration Time	$t_{ZQINIT}$	min	1							$\mu$ s
Long Calibration Time	$t_{ZQCL}$	min	360							ns
Short Calibration Time	$t_{ZQCS}$	min	90							ns
Calibration Reset Time	$t_{ZQRESET}$	min	max(50ns, 3n CK)							ns
Read Parameters										
DQS output access time from CK_t/CK_c	$t_{DQSK}$	min	2500							ps
		max	5500							
DQSK delta short	$t_{DQSKDS}$	max	190	220	243	265	298	330	450	ps
DQSK delta medium	$t_{DQSKDM}$	max	435	511	552	593	637	680	900	ps
DQSK delta long	$t_{DQSKDL}$	max	525	614	674	733	827	920	1200	ps
DQS-DQ skew	$t_{DQSQ}$	max	115	135	150	165	185	200	240	ps
DQS Output High Pulse Width	$t_{QSH}$	min	$t_{CH(abs)} - 0.05$							$t_{CK(avg)}$
DQS Output Low Pulse Width	$t_{QSL}$	min	$t_{CL(abs)} - 0.05$							$t_{CK(avg)}$
DQ/DQS output hold time from DQS	$t_{QH}$	min	$\min(t_{QSH}, t_{QSL})$							ps
Read preamble	$t_{RPRE}$	min	0.9							$t_{CK(avg)}$
Read postamble	$t_{RPST}$	min	0.3							$t_{CK(avg)}$
DQS low-Z from clock	$t_{LZ(DQS)}$	min	$t_{DQSK(min)} - 300$							ps
DQ low-Z from clock	$t_{LZ(DQ)}$	min	$t_{DQSK(min)} - 300$							ps
DQS high-Z from clock	$t_{HZ(DQS)}$	max	$t_{DQSK(max)} - 100$							ps
DQ high-Z from clock	$t_{HZ(DQ)}$	max	$t_{DQSK(max)} - (1.4 \times t_{DQSQ(max)})$							ps



Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	MT/s
Max. Frequency		~	933	800	733	667	600	533	400	MHz
Write Parameters										
DQ and DM input hold time ( $V_{REF}$ based)	$t_{DH}$	min	130	150	165	175	195	210	270	ps
DQ and DM input setup time ( $V_{REF}$ based)	$t_{DS}$	min	130	150	165	175	195	210	270	ps
DQ and DM input pulse width	$t_{DIPW}$	min	0.35							$t_{CK}(avg)$
Write command to 1st DQS latching transition	$t_{DQSS}$	min	0.75							$t_{CK}(avg)$
		max	1.25							$t_{CK}(avg)$
DQS input high-level width	$t_{DQSH}$	min	0.4							$t_{CK}(avg)$
DQS input low-level width	$t_{DQSL}$	min	0.4							$t_{CK}(avg)$
DQS falling edge to CK setup time	$t_{DSS}$	min	0.2							$t_{CK}(avg)$
DQS falling edge hold time from CK	$t_{DSH}$	min	0.2							$t_{CK}(avg)$
Write postamble	$t_{WPST}$	min	0.4							$t_{CK}(avg)$
Write preamble	$t_{WPRE}$	min	0.8							$t_{CK}(avg)$
CKE Input Parameters										
CKE min. pulse width (high and low pulse width)	$t_{CKE}$	min	max(7.5ns, 3n CK)							ns
CKE input setup time	$t_{ISCKE}$	min	0.25							$t_{CK}(avg)$
CKE input hold time	$t_{IHCKE}$	min	0.25							$t_{CK}(avg)$
Command path disable delay	$t_{CPDED}$	min	2							$t_{CK}(avg)$
Command Address Input Parameters										
Address & control input setup time ( $V_{REF}$ based)	$t_{ISCA}$	min	130	150	165	175	200	220	290	ps
Address & control input hold time ( $V_{REF}$ based)	$t_{IHCA}$	min	130	150	165	175	200	220	290	ps
CS_n input setup time ( $V_{REF}$ based)	$t_{ISCS}$	min	230	270	280	290	320	340	410	ps
CS_n input hold time ( $V_{REF}$ based)	$t_{IHCS}$	min	230	270	280	290	320	340	410	ps
Address & control input pulse width	$t_{IPWCA}$	min	0.35							$t_{CK}(avg)$
CS_n input pulse width	$t_{IPWCS}$	min	0.7							$t_{CK}(avg)$
Boot Parameters (10 MHz - 55 MHz)										
Clock Cycle Time	$t_{CKb}$	max	100							ns
		min	18							
CKE input setup time	$t_{ISCKEb}$	min	2.5							ns
CKE input hold time	$t_{IHCKEb}$	min	2.5							ns
Address & control input setup time	$t_{ISb}$	min	1150							ps
Address & control input hold time	$t_{IHb}$	min	1150							ps
DQS Output data access time from CK_t/CK_c	$t_{DQSCkb}$	min	2.0							ns
		max	10.0							
Data strobe edge to output data edge	$t_{DQSQb}$	max	1.2							ns

Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	MT/s
Max. Frequency		~	933	800	733	667	600	533	400	MHz
Mode Register Parameters										
Mode Register Write command period	$t_{MRW}$	min	10							$t_{CK}(avg)$
Mode Register Read command period	$t_{MRR}$	min	4							$t_{CK}(avg)$
Additional time after $t_{XP}$ has expired until MRR command may be issued	$t_{MRRi}$	min	$t_{RCD(MIN)}$							ns
Core Parameters										
Read Latency	RL	min	14	12	11	10	9	8	6	$t_{CK}(avg)$
Write Latency (set A)	WL	min	8	6	6	6	5	4	3	$t_{CK}(avg)$
Write Latency (set B)	WL	min	11	9	9	8				
ACT to ACT command period	$t_{RC}$	min	$t_{RAS} + t_{RPab}$ (with all-bank Precharge)							ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	$t_{CKESR}$	min	max(15ns, 3n CK)							ns
Self refresh exit to next valid command delay	$t_{XSR}$	min	max( $t_{RFCab} + 10ns$ , 2n CK)							ns
Exit power down to next valid command delay	$t_{XP}$	min	max(7.5ns, 3n CK)							ns
CAS to CAS delay	$t_{CCD}$	min	4							$t_{CK}(avg)$
Internal Read to Precharge command delay	$t_{RTP}$	min	max(7.5ns, 4n CK)							ns
RAS to CAS Delay	$t_{RCD}$	min	max(18ns, 3n CK)							ns
Row Precharge Time (single bank)	$t_{RPpb}$	min	max(18ns, 3n CK)							ns
Row Precharge Time (all banks)	$t_{RPab}$	min	max(21ns, 3n CK)							ns
Row Active Time	$t_{RAS}$	min	max(42ns, 3n CK)							ns
		max	70							$\mu s$
Write Recovery Time	$t_{WR}$	min	max(15ns, 4n CK)							ns
Internal Write to Read command delay	$t_{WTR}$	min	max(7.5ns, 4n CK)							ns
Active bank A to Active bank B	$t_{RRD}$	min	max(10ns, 2n CK)							ns
Four Bank Activate window	$t_{FAW}$	min	max(50ns, 8n CK)							ns
Minimum Deep Power Down time	$t_{DPD}$	min	500							$\mu s$
ODT Parameters										
Asynchronous $R_{TT}$ turn-on delay from ODT input	$t_{ODTon}$	min	1.75							ns
		max	3.5							
Asynchronous $R_{TT}$ turn-off delay from ODT output	$t_{ODToff}$	min	1.75							ns
		max	3.5							
Automatic $R_{TT}$ turn-on delay after READ data	$t_{AODTon}$	max	$t_{DQSCk} + 1.4 \times t_{DQSQ,max} + t_{CK}(avg,min)$							ps

Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	MT/s
Max. Frequency		~	933	800	733	667	600	533	400	MHz
ODT Parameters										
Asynchronous R <sub>TT</sub> turn-on delay from ODT input	t <sub>ODTon</sub>	min	1.75							ns
		max	3.5							
Asynchronous R <sub>TT</sub> turn-off delay from ODT output	t <sub>ODToff</sub>	min	1.75							ns
		max	3.5							
Automatic R <sub>TT</sub> turn-on delay after READ data	t <sub>AODTon</sub>	max	t <sub>DQsck</sub> + 1.4 × t <sub>DQs0,max</sub> + t <sub>CK(avg,min)</sub>							ps
Automatic R <sub>TT</sub> turn-off delay after READ data	t <sub>AODToff</sub>	min	t <sub>DQsck,min</sub> - 300							ps
R <sub>TT</sub> disable delay from power down, self refresh, and deep power down entry	t <sub>ODTd</sub>	max	12							ns
R <sub>TT</sub> enable delay from power down, self refresh exit	t <sub>ODTe</sub>	max	12							ns
CA Training Parameters										
First CA calibration command after CA calibration mode is programmed	t <sub>CAMRD</sub>	min	20							t <sub>CK</sub> (avg)
First CA calibration command after CKE is LOW	t <sub>CAENT</sub>	min	10							t <sub>CK</sub> (avg)
CA calibration exit command after CKE is HIGH	t <sub>CAEXT</sub>	min	10							t <sub>CK</sub> (avg)
CKE LOW after CA calibration mode is programmed	t <sub>CACKEL</sub>	min	10							t <sub>CK</sub> (avg)
CKE HIGH after the last CA calibration results are driven	t <sub>CACKEH</sub>	min	10							t <sub>CK</sub> (avg)
Data out delay after CA training calibration command is programmed	t <sub>ADR</sub>	max	20							ns
MRW CA exit command to DQ tri-state	t <sub>MRZ</sub>	min	3							ns
CA calibration command to CA calibration command delay	t <sub>CACD</sub>	min	RU(t <sub>ADR</sub> /t <sub>CK</sub> ) + 2							t <sub>CK</sub> (avg)
Write Leveling Parameters										
DQS <sub>t</sub> /DQS <sub>c</sub> delay after write leveling mode is programmed	t <sub>WLDQSEN</sub>	min	25							ns
		max	--							
First DQS <sub>t</sub> /DQS <sub>c</sub> edge after write leveling mode is programmed	t <sub>WLMRD</sub>	min	40							ns
		max	--							
Write leveling output delay	t <sub>WLO</sub>	min	0							ns
		max	20							
Write leveling hold time	t <sub>WLH</sub>	min	150	175	190	205				ps
Write leveling setup time	t <sub>WLS</sub>	min	150	175	190	205				ps
Mode Register set command delay	t <sub>MRD</sub>	min	max(14ns, 10n CK)							ns
		max	--							

Parameter	Symbol	min/max	LPDDR3							Unit
			1866	1600	1466	1333	1200	1066	800	MT/s
Max. Frequency		~	933	800	733	667	600	533	400	MHz
Temperature Derating										
DQS output access time from CK_t/CK_c (derated)	t <sub>DQSCk</sub>	max	5620							ps
RAS to CAS delay (derated)	t <sub>RCD</sub>	min	t <sub>RCD</sub> + 1.875							ns
ACT to ACT command period (derated)	t <sub>RC</sub>	min	t <sub>RC</sub> + 1.875							ns
Row Active Time (derated)	t <sub>RAS</sub>	min	t <sub>RAS</sub> + 1.875							ns
Row Precharge Time (derated)	t <sub>RP</sub>	min	t <sub>RP</sub> + 1.875							ns
Active bank A to Active bank B (derated)	t <sub>RRD</sub>	min	t <sub>RRD</sub> + 1.875							ns

## 5 Block Diagram

### 5.1 X32 : 4 Banks

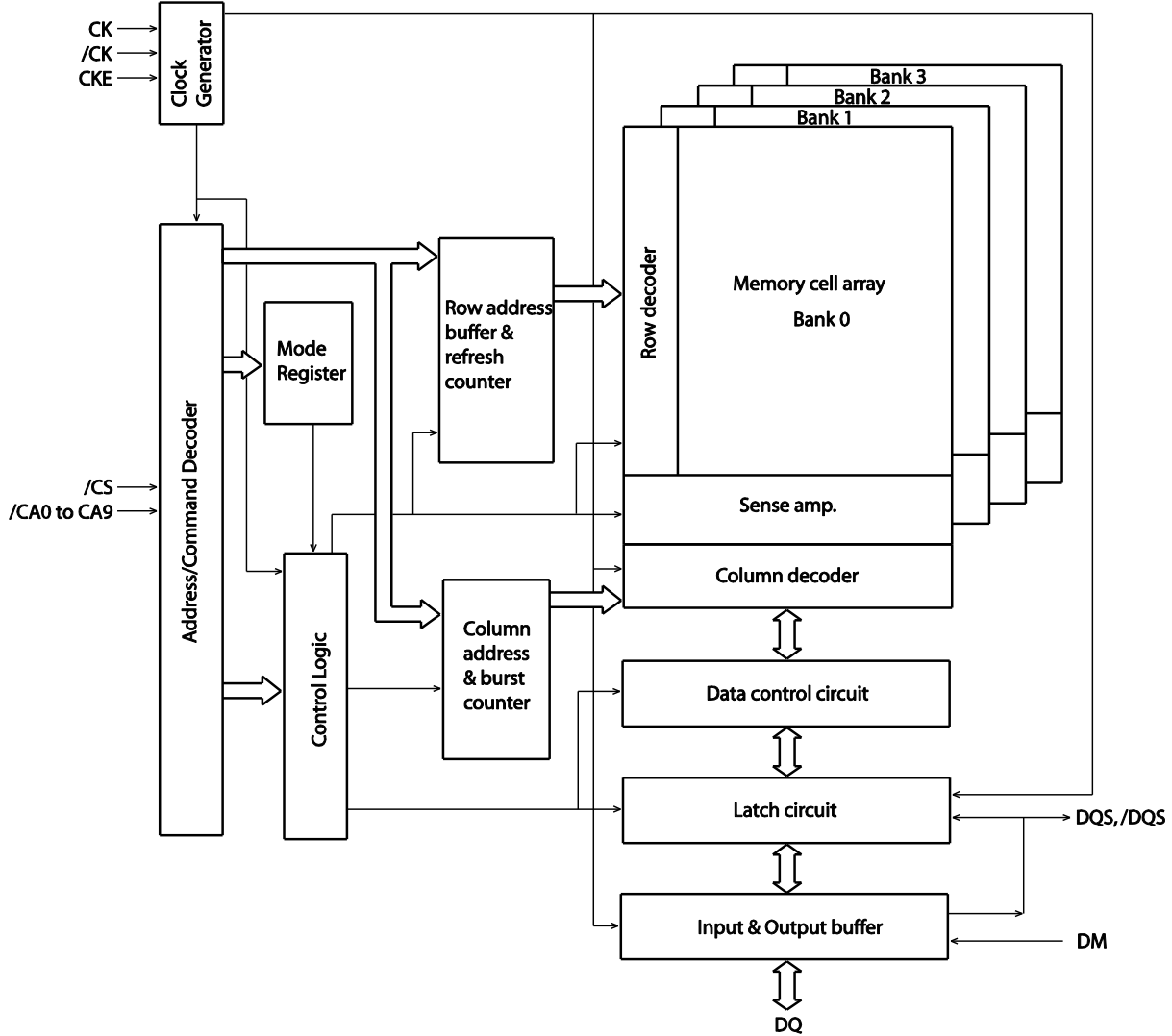


Figure 2. Block Diagram of X32

## 6 Pin Function

### 6.1 *CK\_t, CK\_c (input pins)*

The CK\_t and the CK\_c are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK\_t rising edge and the CK\_c falling edge. When in a read operation, DQSs and DQs are referred to the cross point of the CK\_t and the CK\_c. When in a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK\_t and the CK\_c. The other input signals are referred at CK\_t rising edge.

### 6.2 *CS\_n (input pin)*

When CS\_n is low, commands and data can be input. When CS\_n is high, all inputs are ignored. However, internal operations (bank activate, burst operations, etc.) are held.

### 6.3 *CA0 to CA9 (input pins)*

These pins define the row & column addresses and operating commands (read, write, etc.) depend on their voltage levels. See "Addressing Table" and "Command operation".

### 6.4 *Address Table*

Page Size	Organization	Row address	Column address
4KB	x 32 bits	R0 to R12	C0 <sup>*1</sup> to C9

Command	DDR CA Pins										CK edge
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
Active	--	--	R8	R9	R10	R11	R12	BA0	BA1	BA2 <sup>*2</sup>	↑
	R0	R1	R2	R3	R4	R5	R6	R7	--	--	↓
Write/Read	--	--	--	--	--	C1	C2	BA0	BA1	BA2 <sup>*2</sup>	↑
	AP <sup>*3</sup>	C3	C4	C5	C6	C7	C8	C9	--	--	↓

Remarks: Rx = row address. Cx = column address

Notes:

1. C0 is not present on the command & address, therefore C0 is implied to be zero.
2. BA0,1 & 2 are bank address signals and define to which bank an activate/read/write/precharge command is being applied. The memory array is divided into banks 0, 1, 2,3,4,5,6 and 7.
3. AP defines the precharge mode when a read command or a write command is issued. If AP = high during a read or write command, auto precharge function is enabled.

### 6.5 Bank Numbering and BA Input Table

x32	BA0	BA1
Bank0	L	L
Bank1	H	L
Bank2	L	H
Bank3	H	H

Remarks: H = VIH, L = VIL.

### 6.6 CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least if CKE changes at the crossing point of the CK<sub>t</sub> rising edge and the CK<sub>c</sub> falling edge with proper setup time  $t_{IS}$ , by the next CK<sub>t</sub> rising edge CKE level must be kept with proper hold time  $t_{IH}$ .

### 6.7 DQ0 to DQ31 (x32) - (input/output pins)

Data are input to and output from these pins.

### 6.8 DQSx, /DQSx (input/ output pins, where x = 0 to 3)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input). Each DQS (/DQS) pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

### 6.9 DM0 to DM3 (input pins)

DM is the reference signals of the data input mask function. DM is sampled at the crossing point of DQS and  $V_{DDQ}/2$ . When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up.

### 6.10 [DM truth table]

Name (Functional)	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:

- Used to mask write data. Provided coincident with the corresponding data.

Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

### 6.11 [DQS and DM Correspondence Table]

Part Number	Organization	DQS	Data Mask	DQ
AD310032C-x	x 32 bits	DQS0, /DQS0	DM0	DQ0 to DQ7
		DQS1, /DQS1	DM1	DQ8 to DQ15
		DQS2, /DQS2	DM2	DQ16 to DQ23
		DQS3, /DQS3	DM3	DQ24 to DQ31

### 6.12 ODT (input pin)

ODT turns on/off termination resistance for each DQ, DQS<sub>t</sub>, DQS<sub>c</sub>, and DM. See 9.3.16.

**6.13  $V_{DD1}, V_{DD2}, V_{SS}, V_{DDQ}, V_{SSQ}$  (power supply)**

$V_{DD1}, V_{DD2}$  and  $V_{SS}$  are power supply pins for internal circuits & command address input buffers.  $V_{DDQ}$  and  $V_{SSQ}$  are power supply pins for the output buffers.



## 7 Command Operation

### 7.1 Command Truth Table

The LPDDR3 RAM recognizes the following commands specified by the CS\_n, CA0, CA1, CA2, CA3 and CKE at the rising edge of the clock.

- CA<sub>xr</sub> refers to the command/address bit x on the rising edge of clock. (↑)
- CA<sub>xf</sub> refers to the command/address bit x on the falling edge of clock. (↓)

Function	Symbol	CKE		/CS	DDR CA Pins										CK edge
		Previous cycle	Current cycle		CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
Mode register write	MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				x	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
Mode register read	MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				x	MA6	MA7	x								
Refresh per bank	REFpb	H	H	L	L	L	H	L	x						↑
				x	x										↓
Refresh all banks	REFab	H	H	L	L	L	H	H	x						↑
				x	x										↓
Self-refresh entry	SELF	H	L	L	L	L	H	x						↑	
		x		x										↓	
Bank activate	ACT	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2 <sup>*2</sup>	↑
				x	R0	R1	R2	R3	R4	R5	R6	R7	x	x	↓
Write	WRIT	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2 <sup>*2</sup>	↑
				x	AP <sup>*1</sup>	C3	C4	C5	C6	C7	C8	C9	x	x	↓
Read	READ	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2 <sup>*2</sup>	↑
				x	AP <sup>*1</sup>	C3	C4	C5	C6	C7	C8	C9	x	x	↓
Precharge	PRE	H	H	L	H	H	L	H	AB	x		BA0	BA1	BA2 <sup>*2</sup>	↑
				x	x										↓
Deep power-down mode entry	DPDEN	H	L	L	H	H	L	x						↑	
		x		x										↓	
No operation	NOP	H	H	L	H	H	H	x						↑	
				x	x										↓
Maintain PD/SREF/DPD	NOP	L	L	L	H	H	H	x						↑	
				x	x										↓
No operation	NOP	H	H	H	x										↑
				x	x										↓
Maintain PD/SREF/DPD	DESL	L	L	H	x										↑
				x	x										↓
Device deselect	DESL	H	H	H	x										↑
				x	x										↓
Power-down mode entry	PDEN	H	L	H	x										↑
		x		x										↓	
Exit power-down/deep power-down mode, self refresh	PDEX, SELFX, DPDX	L	H	H	x										↑
		x		x										↓	

Remarks: H = V<sub>IH</sub>, L = V<sub>IL</sub>, x = V<sub>IH</sub> or V<sub>IL</sub>, Rx = row address, Cx = column address, AB = all banks or selected bank precharge.

Notes:

1. AP high during a read or write command indicates that an auto precharge will occur to the bank associated with the read or write command.
2. Bank selects (BA0,1 & 2) determine which bank is to be operated upon. BA2 is used for x16 and don't care for x32.
3. Self-refresh exit and deep power-down exit are asynchronous.

CS<sub>n</sub> and CKE are sampled at the rising edge of clock.  
V<sub>REF</sub> must be maintained during self-refresh and deep power-down operation.

## 7.2 Register Commands [MRR/MRW]

The register commands include both a mode register read (MRR) and a mode register write (MRW) command. The protocol provides support for a total of up to 256 8-bit registers, which will be either read-only, write-only, or both readable and writeable by the memory controller.

## 7.3 Refresh Commands [REF]

The refresh commands include an All Banks refresh command, and a self-refresh command. Entry into self-refresh mode will occur upon the transition of CKE from high to low.

## 7.4 Activate Command [ACT]

Only CA0r and CA1r are needed to encode this command. The remaining bits in the CA map specify the row and bank address.

## 7.5 Read/Write Commands [READ/WRITE]

The read and write commands indicate whether a read or write is desired. CA0r, CA1r, and CA2r are needed to encode either command. The remaining bits in the CA map are used to indicate the column address. A bit to indicate whether an auto precharge is desired is provided and is registered on CA0f of both read and write commands. Two bits in the read and write command encoding have been specified as Reserved for Future Use (RFU).

## 7.6 Precharge Commands [PRE]

The Precharge command requires that the bank be specified at command time only when the auto precharge bit indicates that an All Bank pre-charge is not desired (I.E. AB (CA4r) = 0). If the All Bank precharge bit is set (I.E. AB (CA4r) = 1), bank information is not required.

## 7.7 Power-down and Deep Power Down [PDEN/DPDEN]

Both power-down and deep power-down modes are supported by the protocol. In normal power-down mode all input and output buffers as well as CK<sub>t</sub> and CK<sub>c</sub> will be disabled. If all banks are precharged prior to entering power-down mode, the device will be said to be in Precharge power-down mode. If at least one bank is open while entering power-down mode, the SDRAM device will be said to be in Active power-down mode.

In Deep power-down mode all input/output buffers, CK<sub>t</sub>, CK<sub>c</sub>, and power to the array will be disabled. The contents of the SDRAM will be lost upon entry into deep power-down mode.

The command for entry into normal power-down mode requires that CS<sub>n</sub> is high, while the command for entry into Deep power-down mode requires that CS<sub>n</sub> be low. In both cases CKE will remain active and will be the mechanism by which the SDRAM is able to exit either power-down modes.

## 7.8 Exit Command [PDEX, DPDX, SELFX]

Exit from self-refresh, power down, or deep power-down modes requires a low to high transition of CKE.

## 7.9 No Operation Command [NOP]

NOP can either be issued using a command when CS<sub>n</sub> is low or by simply deselecting CS<sub>n</sub>.

**7.10 CKE Truth Table**

Current state <sup>*2</sup>	CKE		Command (n) <sup>*3</sup>	Operation (n) <sup>*3</sup>	Notes
	Previous cycle (n-1) <sup>*1</sup>	Current cycle (n) <sup>*1</sup>	/CS, CA0r to CA3r		
Active/Idle power-down	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Power-down exit	4
Deep power-down entry	L	L	×	Maintain power-down	8
	L	H	DESL or NOP	Deep power-down exit	
Self-refresh	L	L	×	Maintain self-refresh	8
	L	H	DESL or NOP	Self-refresh exit	4, 7
Bank Active	H	L	DESL or NOP	Active power down entry	4
All banks idle	H	L	DESL or NOP	Precharge power down entry	4
	H	L	SELF	Self-refresh entry	5
Other	H	H	Refer to the Command Truth Table		6

 Remark: H = V<sub>IH</sub>, L = V<sub>IL</sub>, × = Don't care

Notes:

1. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the LPDDR3 RAM immediately prior to clock edge n.
3. Command (n) is the command registered at clock edge n, and operation (n) is a result of Command (n).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. Self-refresh mode can only be entered from the all banks idle state.
6. Must be a legal command as defined in the command truth table.
7. Valid commands for deep power-down exit and power-down exit and self-refresh exit are NOP and DESL only.
8. Deep power-down, power-down and self-refresh cannot be entered while read/write operations, mode register read/write or precharge operations are in progress.
9. V<sub>REF</sub> must be maintained during self-refresh operation.
10. Clock frequency may be changed or stopped during the active power-down or idle power-down state.

### 8 Simplified State Diagram

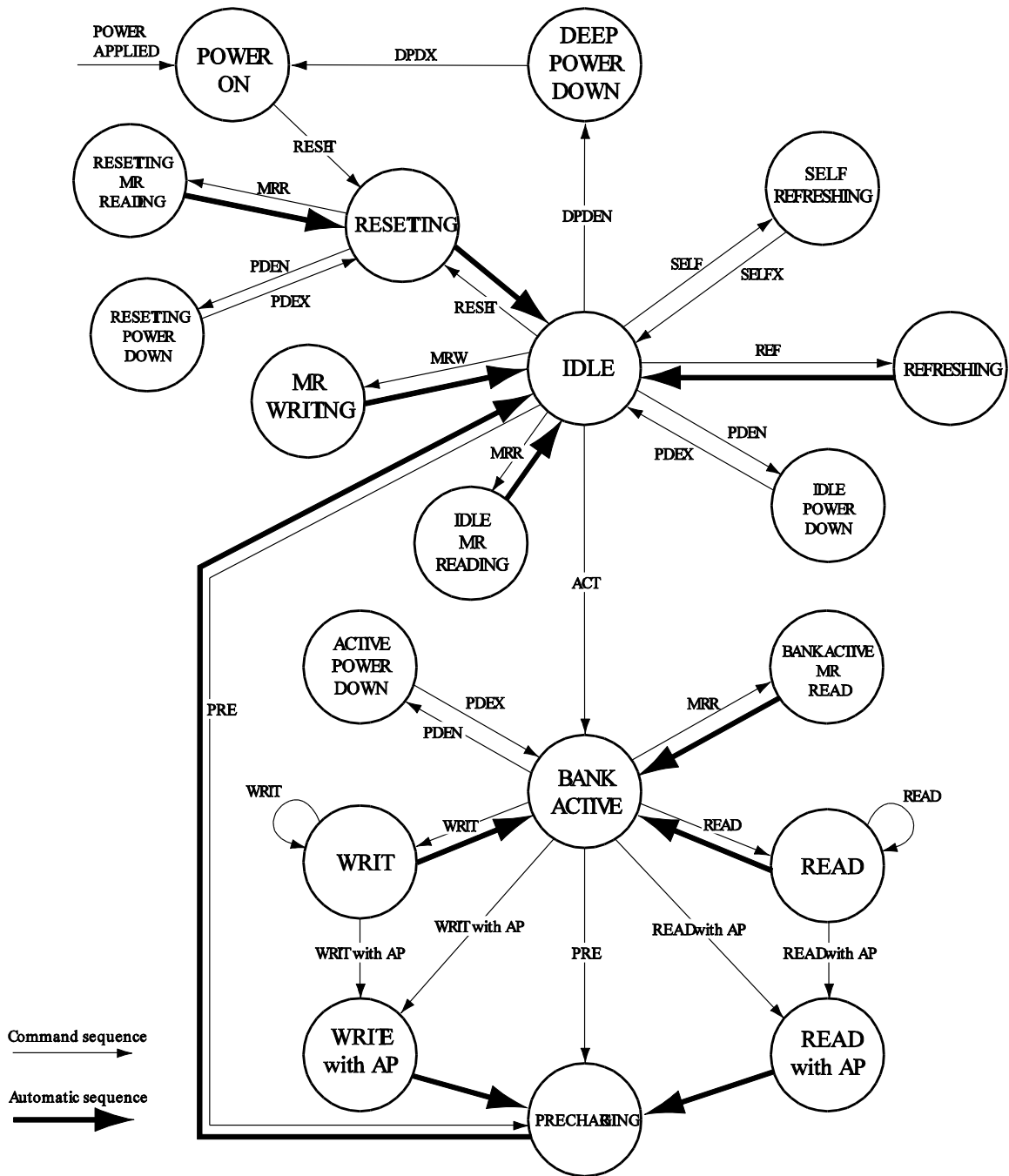


Figure 3 Simplified State Diagram

## 9 Operation of the LPDDR3 RAM

Read and write accesses to the LPDDR3 RAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of eight in a programmed sequence. Accesses begin with the registration of an activate command, which is then followed by a read or write command. The address and BA bits registered coincident with the activate command is used to select the row and bank to be accessed (BA0 & 1 selects the bank; R0 to R12 selects the row). The address bits registered coincident with the read or write command are used to select the starting column location for the burst access.

Prior to normal operations, the LPDDR3 RAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

### 9.1 LPDDR3 RAM Power-On and Initialization Sequence

#### 9.1.1 Power Ramp and Device Initialization

##### **Power Ramp**

While applying power (after  $T_a$ ), CKE shall be held at a logic low level ( $\leq 0.2 \times V_{DD2}$ ), all other inputs shall be between  $V_{IL}$  (min) and  $V_{IH}$  (max). The LPDDR3 RAM device will only guarantee that outputs are in a high impedance state while CKE is held low. On or before the completion of the power ramp ( $T_b$ ) CKE must be held low. Voltage levels at I/Os and outputs must be between  $V_{SSQ}$  and  $V_{DDQ}$  and Inputs must be between  $V_{SS}$  and  $V_{DD2}$  during voltage ramp time to avoid latch-up.

The following conditions apply:

- $T_a$  is the point where any power supply first reaches 300mV.
- After  $T_a$  is reached,  $V_{DD1}$  must be greater than  $V_{DD2} - 200\text{mV}$ .
- After  $T_a$  is reached,  $V_{DD1}$  and  $V_{DD2}$  must be greater than  $V_{DDQ} - 200\text{mV}$ .
- After  $T_a$  is reached,  $V_{REF}$  must always be less than all other supply voltages.
- The voltage difference between any of  $V_{SS}$ , and  $V_{SSQ}$  pins may not exceed 100mV.
- $T_b$  is the point when all supply and reference voltages are within their respective min/max operating conditions.
- Power ramp duration  $t_{INIT0}$  ( $T_b - T_a$ ) must be no greater than 20ms.

Beginning at  $T_b$ , CKE must remain LOW for at least  $t_{INIT1} = 100\text{ns}$ , after which it may be asserted HIGH. Clock must be stable at least  $t_{INIT2} = 5 t_{CK}$  prior to the first CKE LOW to HIGH transition ( $T_c$ ). CKE, CS\_n and CA inputs must observe setup and hold time ( $t_{IS}$ ,  $t_{IH}$ ) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

If any MRR commands are issued, the clock period must be within the range defined for  $t_{CKb}$ . MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example,  $t_{DQSCk}$ ) could have relaxed timings (such as  $t_{DQSCkb}$ ) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least  $t_{INIT3}(T_d)$ . The ODT input signal may be in undefined state until  $t_{IS}$  before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of  $t_{ZQINIT}$ .

##### **Reset Command**

After  $t_{INIT3}$  is satisfied, a MRW (Reset) command shall be issued ( $T_d$ ). Wait for at least  $t_{INIT4} = 1\mu\text{s}$  while keeping CKE asserted and issuing NOPs. Optionally PRECHARGE ALL command can be issued prior to the MRW RESET command.

##### **Mode Register Reads and Device Auto-Initialization (DAI) polling**

After  $t_{INIT4}$  is satisfied ( $T_e$ ), only MRR commands (including power-down entry/exit) are allowed. After  $T_e$ , CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. CA Training may only begin after time  $T_f$ . User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after  $t_{INIT5}(\text{max})$  has expired (whether or not DAI bit has been read by MRR command). As the memory output buffers are not properly configured by  $T_e$ , some AC parameters must have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR0.DAI) is set to “ready” by the memory device, the device is in idle state (Tf). DAI status can be determined by an MRR command to MR0. The device sets the DAI bit no later than  $t_{INIT5}$  after the Reset command. The controller must wait at least  $t_{INIT5(max)}$  or until the DAI bit is set before proceeding.

### ***ZQ Calibration***

If CA Training is not required, the MRW initialization calibration (ZQ\_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration (ZQ\_CAL) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ\_CAL commands. The device is ready for normal operation after  $t_{ZQINIT}$ .

### ***Normal Operation***

After  $t_{ZQINIT}$  (Tg), MRW commands must be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency may be changed using the procedure described in section Input Clock Stop and Frequency Change during Power-Down of this specification.

### 9.1.2 Timing Parameters for Initialization

Symbol	Value		Unit	Test Condition
	min.	max.		
$t_{INIT0}$	--	20	ms	Maximum Power Ramp Time
$t_{INIT1}$	100	--	ns	Minimum CKE low time after completion of power ramp
$t_{INIT2}$	5	--	tCK	Minimum stable clock before first CKE high
$t_{INIT3}$	200	--	$\mu$ s	Minimum Idle time after first CKE assertion
$t_{INIT4}$	1	--	$\mu$ s	Minimum Idle time after Reset command
$t_{INIT5}$	--	10	$\mu$ s	Maximum duration of Device Auto-Initialization
$t_{ZQINIT}$	1	--	$\mu$ s	ZQ initial calibration
$t_{CKBOOT}$	18	100	ns	Clock cycle time during boot

[See Figure 2 in JEDEC Standard No. 209-3B]

#### Initialization After RESET (without power ramp)

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

#### Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ( $\leq 0.2 \times V_{DD2}$ ); all other inputs must be between  $V_{ILmin}$  and  $V_{IHmax}$ .

The device outputs remain at High-Z while CKE is held LOW.

DQ, DM, DQS\_t, and DQS\_c voltage levels must be between  $V_{SSQ}$  and  $V_{DDQ}$  during the power-off sequence to avoid latch-up.

CK\_t, CK\_c, CS\_n, and CA input levels must be between  $V_{SS}$  and  $V_{DD2}$  during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off (see the following Table).

Between...	Applicable Conditions
Tx and Tz	$V_{DD1}$ must be greater than $V_{DD2} - 200mV$
Tx and Tz	$V_{DD1}$ must be greater than $V_{DDQ} - 200mV$
Tx and Tz	$V_{REF}$ must always be less than all other supply voltages

The voltage difference between any of  $V_{SS}$  and  $V_{SSQ}$  pins must not exceed 100mV.

#### Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system..

#### Power-up, Initialization, and Power-off (cont'd)

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled.  $V_{DD1}$  and  $V_{DD2}$  must decrease with a slope lower than  $0.5 V/\mu$ s between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Symbol	Value		Unit	Comment
	min.	max.		
$t_{POFF}$	--	2	s	Maximum Power-Off ramp time



9.2 Programming the Mode Register

9.2.1 Mode Register Assignment

MR No.	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Remark	
0	00h	Device Info.	R	RL3	WL (Set B)	(RFU)	00	(RFU)	(RFU)		DAI	See MR0	
1	01h	Device Feature 1	W	nWR (for AP)			(RFU)	BL				See MR1	
2	02h	Device Feature 2	W	WR Lev	WL Select	(RFU)	nWRE	RL & WL				See MR2	
3	03h	I/O Config-1	W	(RFU)			DS				See MR3		
4	04h	Refresh Rate	R	TUF	(RFU)			Refresh Rate				See MR4	
5	05h	Basic Config-1	R	Company ID									See MR5
6	06h	Basic Config-2	R	Revision ID1									See MR6
7	07h	Basic Config-3	R	Revision ID2									See MR7
8	08h	Basic Config -4	R	I/O Width		Density			Type			See MR8	
9	09h	Test Mode	W	Vendor-Specific Test Mode									See MR9
10	0Ah	IO Calibration	W	Calibration Code									See MR10
11	0Bh	ODT Feature	W	(RFU)				PD CTL	DQ ODT			See MR11	
12:15	0Ch TO 0Fh	Reserved		(RFU)									
16	10h	PASR_Bank	W	Bank Mask									See MR16
17	11h	PASR_Seg	W	Segment Mask									See MR17
18:31	12h to 1Fh	Reserved		(RFU)									
32	20h	DQ Calibration Pattern A	R	See DQ Calibration									See MR32
40	28h	DQ Calibration Pattern B	R	See DQ Calibration									See MR40
41	29h	CA Training 1	W	See CA Training									See MR41
42	2Ah	CA Training 2	W	See CA Training									See MR42
48	30h	CA Training 3	W	See CA Training									See MR43
49:62	31h to 3Eh	Reserved		(RFU)									
63	3FH	Reset	W	x									See MR63
64:255	40h to FFh	Reserved		(RFU)									

Notes:

1. RFU bits shall be set to '0' during mode register writes.
2. RFU bits shall be read as '0' during mode register reads.
3. All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS\_t, DQS\_c shall be toggled.
4. All mode registers that are specified as RFU shall not be written.
5. See vendor device datasheets for details on vendor-specific mode registers.
6. Writes to read-only registers shall have no impact on the functionality of the device.

**MR0 Device Information**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
<b>MR0</b>	RL3	WL (Set B)	(RFU)	RZQI (optional)		(RFU)		DAI

Device Auto-Initialization	Read-only	OP[0]	0	DAI complete	
			1	DAI still in progress	
RZQI	Read-only	OP[4:3]	00	RZQ self test not supported	1-4
WL (Set B) Support	Read-only	OP[6]	1	DRAM supports WL (Set B)	supported
RL3 Option Support	Read-only	OP[7]	1	DRAM supports RL=3, nWR=3, WL=1 for frequencies ≤ 166	supported

**MR1 Device Feature**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
<b>MR1</b>	nWR (for AP)		(RFU)			BL		

BL	Write-only	OP[2:0]	011	BL8 (default)	
			others	reserved	
nWR	Write-only	OP[7:5]	If nWRE (MR2 OP[4]) = 0		1
			001	nWR=3 (optional)	
			100	nWR=6	
			110	nWR=8	
			111	nWR=9	
			If nWRE (MR2 OP[4]) = 1		
			000	nWR=10 (default)	
			001	nWR=11	
			010	nWR=12	
			100	nWR=14	
			110	nWR=16	
			others	reserved	

Notes:

1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by  $RU(tWR/tCK)$ .

Burst Cycle Number and Burst Address											
C2	C1	C0	BL	1	2	3	4	5	6	7	8
0	0	0	8	0	1	2	3	4	5	6	7
0	1	0		2	3	4	5	6	7	0	1
1	0	0		4	5	6	7	0	1	2	3
1	1	0		6	7	0	1	2	3	4	5

Notes:

1. C0 input is not present on CA bus. It is implied zero.
2. The burst address represents C2-C0.

**MR2 Device Feature**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR2	WR Lev	WL Select	(RFU)	nWRE	RL & WL			

Feature	Access	OP	If OP[6] = 0 (WL Set A, default)	
			OP	Description
RL & WL	Write-only	OP[3:0]	0001	RL = 3 / WL = 1 ( $\leq$ 166 MHz)
			0100	RL = 6 / WL = 3 ( $\leq$ 400 MHz)
			0110	RL = 8 / WL = 4 ( $\leq$ 533 MHz)
			0111	RL = 9 / WL = 5 ( $\leq$ 600 MHz)
			1000	RL = 10 / WL = 6 ( $\leq$ 677 MHz, default)
			1001	RL = 11 / WL = 6 ( $\leq$ 733 MHz)
			1010	RL = 12 / WL = 6 ( $\leq$ 800 MHz)
			1100	RL = 14 / WL = 8 ( $\leq$ 933 MHz)
			others	reserved
			If OP[6] = 1 (WL Set B)	
			0001	RL = 3 / WL = 1 ( $\leq$ 166 MHz)
			0100	RL = 6 / WL = 3 ( $\leq$ 400 MHz)
			0110	RL = 8 / WL = 4 ( $\leq$ 533 MHz)
			0111	RL = 9 / WL = 5 ( $\leq$ 600 MHz)
			1000	RL = 10 / WL = 8 ( $\leq$ 677 MHz, default)
			1001	RL = 11 / WL = 9 ( $\leq$ 733 MHz)
1010	RL = 12 / WL = 9 ( $\leq$ 800 MHz)			
1100	RL = 14 / WL = 11 ( $\leq$ 933 MHz)			
others	reserved			
nWRE	Write-only	OP[4]	0	enable nWR programming $\leq$ 9
			1	enable nWR programming $>$ 9 (default)
WL Select	Write-only	OP[6]	0	Select WL Set A (default)
			1	Select WL Set B
WR Leveling	Write-only	OP[7]	0	disable (default)
			1	enable

**MR3 I/O Configuration 1**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR3	(RFU)				DS			

DS	Write-only	OP[3:0]	OP[3:0]	Value
DS	Write-only	OP[3:0]	0001	34.3Ω typical pull-down/pull-up
			0010	40Ω typical pull-down/pull-up (default)
			0011	48Ω typical pull-down/pull-up
			0100	60Ω typical pull-down/pull-up
			0110	80Ω typical pull-down/pull-up
			1001	34.3Ω typical pull-down, 40Ω typical pull-up
			1010	40Ω typical pull-down, 48Ω typical pull-up
			1011	34.3Ω typical pull-down, 48Ω typical pull-up
			others	reserved

**MR4 Device Temperature**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR4	TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP[2:0]	OP[2:0]	Value
SDRAM Refresh Rate	Read-only	OP[2:0]	000	SDRAM Low temperature operating limit exceeded
			001	$4x t_{REFI}$ , $4x t_{REFIPD}$ , $4x t_{REFW}$
			010	$2x t_{REFI}$ , $2x t_{REFIPD}$ , $2x t_{REFW}$
			011	$1x t_{REFI}$ , $1x t_{REFIPD}$ , $1x t_{REFW}$
			100	$0.5x t_{REFI}$ , $0.5x t_{REFIPD}$ , $0.5x t_{REFW}$ , do not de-rate SDRAM AC timing
			101	$0.25x t_{REFI}$ , $0.25x t_{REFIPD}$ , $0.25x t_{REFW}$ , do not de-rate SDRAM AC timing
			110	$0.25x t_{REFI}$ , $0.25x t_{REFIPD}$ , $0.25x t_{REFW}$ , de-rate SDRAM AC timing
			111	SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP[7]	0	OP[2:0] value has not changed since last read of MR4
			1	OP[2:0] value has changed since last read of MR4

Notes :

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up. OP[2:0] bits are undefined after power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. SDRAM might not operate properly when OP[2:0] = 3'b000 or 3'b111.
6. For specified operating temperature range and maximum operating temperature refer to 4.2.
7. LPDDR3 devices shall be de-rated by adding 1.875ns to the following core timing parameters:  $t_{RCD}$ ,  $t_{RC}$ ,  $t_{RAS}$ ,  $t_{RP}$ , and  $t_{RRD}$ .  $t_{DQSQCK}$  shall be de-rated according to the  $t_{DQSQCK}$  de-rating in **AC Characteristics**. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. See 9.3.15 for information on the recommended frequency of reading MR4.

**MR5 Basic Configuration 1**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR5	LPDDR3 Manufacturer ID							

LPDDR3 Manufacturer ID	Read-only	OP[7:0]	11111101	AP Memory	
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**MR6 Basic Configuration 2**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR6	Revision ID1							

Revision ID1	Read-only	OP[7:0]	00000000	A-version	
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**MR7 Basic Configuration 3**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR7	Revision ID2							

Revision ID2	Read-only	OP[7:0]	00000000	A-version	
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**MR8 Basic Configuration**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR8	I/O Width	Density			Type			

Type	Read-only	OP[1:0]	11	S8 SDRAM	512Mb is specially configured
			others	reserved	
Density	Read-only	OP[5:2]	0011	512Mb	
			0100	1Gb	
			others	reserved	
I/O Width	Read-only	OP[7:6]	00	x32	
			01	x16	
			others	reserved	

**MR9 Test Mode**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR9	vendor-specific test mode							

Failed Die	Read-only	OP[4]	0	Pass (default)	
			1	Fail	
Tested Die		OP[5]	0	Reserved	
			1	Reserved	

**MR10 Calibration**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR10	Calibration Code							

Calibration Code	Write-only	OP[7:0]	'hFF	Calibration command after initialization	
			'hAB	Long calibration	
			'h56	Short calibration	
			'hC3	ZQ Reset	
			others	reserved	

Notes:

- Host processor shall not write MR10 with “Reserved” values.
- LPDDR3 devices shall ignore calibration command when a “Reserved” value is written into MR10.
- See AC timing table for the calibration latency.
- If ZQ is connected to V<sub>SS</sub> through R<sub>ZQ</sub>, either the ZQ calibration function (see 0) or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V<sub>DD2</sub>, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
- LPDDR3 devices that do not support calibration shall ignore the ZQ Calibration command.
- Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

**MR11 ODT Control**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR11	RFU					PD CTL	DQ ODT	

DQ ODT	Write-only	OP[1:0]	00	Disable (default)	
			01	R <sub>ZQ</sub> /4 (see Note 1)	
			10	R <sub>ZQ</sub> /2	
			11	R <sub>ZQ</sub> /1	
PD Control	Write-only	OP[2]	0	ODT disabled by DRAM during power down (default)	
			1	ODT enabled by DRAM during power down	

Notes :

- R<sub>ZQ</sub>/4 shall be supported for LPDDR3-1866 and LPDDR3-2133 devices. R<sub>ZQ</sub>/4 support is optional for LPDDR3-1333 and LPDDR3-1600 devices. Consult manufacturer specifications for R<sub>ZQ</sub>/4 support for LPDDR3-1333 and LPDDR3-1600.

**MR16 PASR Bank Mask**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR16	Bank Mask							

Bank [7:0] Mask	Write-only	OP[7:0]	0	refresh enabled to the bank (=unmasked, default)
			1	refreshed blocked (=masked)

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
0	XXX1XXXX	Bank 4
1	XX1XXXXX	Bank 5
2	X1XXXXXX	Bank 6
3	1XXXXXXX	Bank 7

**MR17 PASR Segment Mask**

OP	Segment Mask	8 Segments/bank	x16/x32
0	XXXXXXX1	Segment 0	x16/x32
1	XXXXXX1X	Segment 1	x16/x32
2	XXXXX1XX	Segment 2	x16/x32
3	XXXX1XXX	Segment 3	x16/x32
0	XXX1XXXX	Segment 4	x16/x32
1	XX1XXXXX	Segment 5	x16/x32
2	X1XXXXXX	Segment 6	x16/x32
3	1XXXXXXX	Segment 7	x16/x32

**MR32 & MR40 DQ Calibration Patterns**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR32	DQ Calibration Pattern "A"							
MR40	DQ Calibration Pattern "B"							

LPDDR3 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern "A") or MR40 (Pattern "B") will return the specified pattern on DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 'b0 during the MRR burst.

		Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Bit Time 4	Bit Time 5	Bit Time 6	Bit Time 7
DQ Calibration Pattern "A"	Read-only	1	0	1	0	1	0	1	0
DQ Calibration Pattern "B"	Read-only	0	0	1	1	0	0	1	1

[See Figure 37 in JEDEC Standard No. 209-3B]

**MR41, MR42 & MR48 CA Training**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR41	CA Training Entry							
MR42	CA Training Exit							
MR48	CA Training Mapping							

CA Training Sequence:

CA Training mode entry (MRW to MR41).

CA Training session: CA0, CA1,...CA8 (see Table 2)

CA to DQ mapping change (MRW to MR48).

Additional CA Training session : Calibrate remaining CA pins (CA4 and CA9) (see Table 3)

CA Training mode exit (MRW to MR42).

[See Figure 44 in JEDEC Standard No. 209-3B]

The LPDDR3 SDRAM may not properly recognize a Mode Register Write command at normal operation frequency before CA Training is completed. Special encodings are provided for CA Training mode enable/disable. MR 41 and MR42 encodings are selected so that rising edge and falling edge values are the same. The LPDDR3 SDRAM will recognize MR41, MR42, and MR48 at normal operation frequency even before CA timing adjustment is finished.

**Table 1: CA Training encodings**

	CLK edge	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9
CA Training mode enable OP='b1010_0100 ('hA4)	Rising Edge	L	L	L	L	H	L	L	H	L	H
	Falling Edge	L	L	L	L	H	L	L	H	L	H
CA Training mode disable OP='b1010_1000 ('hA8)	Rising Edge	L	L	L	L	L	H	L	H	L	H
	Falling Edge	L	L	L	L	L	H	L	H	L	H
CA Training mapping OP='b1100_0000 ('hC0)	Rising Edge	L	L	L	L	L	L	L	L	H	H
	Falling Edge	L	L	L	L	L	L	L	L	H	H

Calibration data will be output through DQ pins. CA to DQ mapping is described in Table 2.

After timing calibration with MR41 is finished, users will issue MRW to MR48 and calibrate remaining CA pins (CA4 and CA9) using (DQ0/DQ1 and DQ8/DQ9) as calibration data output pins (see Table 3).

CA Training timing values are specified in **AC Characteristics**.

**Table 2: CA to DQ mapping (via MR41)**

	CLK edge	CA0	CA1	CA2	CA3	CA5	CA6	CA7	CA8
CA Training mode enabled with MR41	Rising Edge	DQ0	DQ2	DQ4	DQ6	DQ8	DQ10	DQ12	DQ14
	Falling Edge	DQ1	DQ3	DQ5	DQ7	DQ9	DQ11	DQ13	DQ15

**Table 3: CA to DQ mapping (via MR48)**

	CLK edge	CA4	CA9
CA Training mode enabled with MR48	Rising Edge	DQ0	DQ8
	Falling Edge	DQ1	DQ9

Note 1: Other DQs must have valid output (either HIGH or LOW)



**MR63 Reset**

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR63	X or 0xFC							

The MRW RESET command brings the device to the device auto-initialization (resetting) state in the power-on initialization sequence. The MRW RESET command can only be issued from an all bank idle state. This command resets all mode registers to their default values. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command.

If the initialization is to be performed at-speed (greater than the recommended boot clock frequency), then CA Training may be necessary to ensure setup and hold timings. Since the MRW RESET command is required prior to CA Training it may be difficult to meet setup and hold requirements. User may however choose the OP code 'hFC. This encoding ensures that no transitions are required on the CA bus between rising and falling clock edge. Prior to CA Training, it is recommended to hold the CA bus stable for one cycle prior to, and once cycle after, the issuance of the MRW RESET command to ensure setup and hold timings on the CA bus.

[See Figure 39 in JEDEC Standard No. 209-3B]

### 9.3 LPDDR3 Command Definitions and Timing Diagrams

#### 9.3.1 Bank Activate Command [ACT]

The bank activate command is issued by holding CS<sub>n</sub> LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 & 1 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any read or write operation can be executed. Immediately after the Bank Activate command, the LPDDR3 RAM can accept a read or write command on the following clock cycle at time t<sub>RCD</sub> after the activate command is sent. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank activation and precharge times are defined as t<sub>RAS</sub> and t<sub>RP</sub>, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the RAS cycle time of the device (t<sub>RC</sub>). The minimum time interval between successive bank activation commands to the different bank is determined by (t<sub>RRD</sub>).

[See Figure 3 in JEDEC Standard No. 209-3B]

#### 9.3.2 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS<sub>n</sub> LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2<sub>r</sub> must also be defined at this time to determine whether the access cycle is a read operation (CA2<sub>r</sub> HIGH) or a write operation (CA2<sub>r</sub> LOW).

The LPDDR3 RAM provides a fast column access operation. A single read or write command will initiate a serial read or write operation on successive clock cycles. Burst interrupts are not allowed. The minimum CAS to CAS delay is defined by t<sub>CCD</sub>.

#### 9.3.3 Burst Read Command [READ]

The Burst READ command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The address inputs, CA5<sub>r</sub> to CA6<sub>r</sub> and CA1<sub>f</sub> to CA7<sub>f</sub>, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the t<sub>DQSCk</sub> delay is measured. The first valid datum is available RL x t<sub>CK</sub> + t<sub>DQSCk</sub> + t<sub>DQSQ</sub> after the rising edge of the clock where the READ command is issued. The data strobe output (DQS) is driven LOW t<sub>RPRE</sub> before valid data (DQ) is driven onto the data bus.

The first bit of the burst is synchronized with the first rising edge of the data strobe (DQS). Each subsequent dataout appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is programmed in the mode registers.

Pin timings are measured relative to the cross point of DQS and its complement, /DQS.

[See Figures 7 - 12 in JEDEC Standard No. 209-3B]

The minimum time from the burst READ command to the burst WRITE command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(t<sub>DQSCkmax</sub>/t<sub>CK</sub>) + BL/2 + 1 – WL.

[See Figure 13 in JEDEC Standard No. 209-3B]

The seamless burst READ operation is supported by enabling a READ command at every 4<sup>th</sup> clock cycle for BL = 8 operation. This operation is allowed regardless of whether accessing same or different banks as long as the accessed banks are activated.

### 9.3.4 **Burst Write Command [WRIT]**

The burst WRITE command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The address inputs determine the starting column address. The first valid data is available Write Latency (WL) x t<sub>CK</sub> + t<sub>DQSS</sub> from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) must be driven for time t<sub>WPRE</sub> as shown in Figure 17 prior to data input. The burst cycle data bits must be applied to the DQ pins t<sub>DS</sub> prior to the associated edge of the DQS and held valid until t<sub>DH</sub> after that edge. Burst data is sampled on successive edges of the DQS until the 8-bit burst length is completed. After a burst WRITE operation, t<sub>WR</sub> must be satisfied before a precharge command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of DQS<sub>t</sub> and its complement, DQS<sub>c</sub>.

[See Figure 15 - 16 in JEDEC Standard No. 209-3B]

#### **t<sub>WPRE</sub> Calculation**

[See Figure 17 in JEDEC Standard No. 209-3B]

#### **t<sub>WPST</sub> Calculation**

[See Figure 18 in JEDEC Standard No. 209-3B]

[See Figure 19 in JEDEC Standard No. 209-3B]

Note 1: The minimum number of clocks from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(t<sub>WTR</sub>/t<sub>CK</sub>)].

Note 2: t<sub>WTR</sub> starts at the rising edge of the clock after the last valid input datum.

[See Figure 20 in JEDEC Standard No. 209-3B]

- Note 1: The seamless burst write operation is supported by enabling a write command every four clocks for BL = 8 operation. This operation is allowed for any activated bank.

#### **Write Data Mask**

On LPDDR3 devices, one write data mask (DM) pin for each data byte (DQ) is supported, consistent with the implementation on LPDDR2 SDRAM. Each DM can mask its respective DQ for any given cycle of the burst. Data mask timings match data bit timing, but are inputs only. Internal data-mask loading is identical to data-bit loading to ensure matched system timing. For data mask timing, see Figure 21.

[See Figure 21 in JEDEC Standard No. 209-3B]

**9.3.5 Precharge Command [PRE]**

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated by having CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bits BA[1:0] are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access t<sub>RPab</sub> after an all-bank PRECHARGE command is issued, or t<sub>RPpb</sub> after a single-bank PRECHARGE command.

To ensure that LPDDR3 devices can meet the instantaneous current demand required to operate, the row-precharge time for an all-bank PRECHARGE (t<sub>RPab</sub>) will be longer than the row PRECHARGE time for a single-bank PRECHARGE (t<sub>RPpb</sub>). Activate to Precharge timing is shown in Figure 3.

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s)
L	L	L	L	Bank 0 only
L	L	L	H	Bank 1 only
L	L	H	L	Bank 2 only
L	L	H	H	Bank 3 only

Remark: H = V<sub>IH</sub>, L = V<sub>IL</sub>, x = V<sub>IH</sub> or V<sub>IL</sub>

**Burst Read Operation Followed by Precharge**

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clocks after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (t<sub>RP</sub>) has elapsed. A PRECHARGE command cannot be issued until after t<sub>RAS</sub> is satisfied. The minimum READ to PRECHARGE spacing must also satisfy a minimum analog time from the rising clock edge that initiates the last 8n prefetch of a READ command. This time is called t<sub>RTP</sub> (Read to Precharge) and begins BL/2 – 4 clock cycles after the READ command. For LPDDR3 READ-to-PRECHARGE timings see Table 4.

[See Figure 22 in JEDEC Standard No. 209-3B]

**Burst Write Operation Followed by Precharge**

For WRITE cycles, a WRITE recovery time (t<sub>WR</sub>) must be provided before a PRECHARGE COMMAND CAN BE ISSUED. This delay is referenced from the last valid burst input data to the completion of the burst WRITE. A PRECHARGE command must not be issued prior to the t<sub>WR</sub> delay. For LPDDR3 WRITE-to-PRECHARGE timings see Table 4.

LPDDR3 devices write data to the array in prefetch multiples (prefetch = 8). An internal WRITE operation can only begin after a prefetch group has been completely latched, so t<sub>WR</sub> starts at prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(t<sub>WR</sub>/t<sub>CK</sub>) clock cycles.

[See Figure 23 in JEDEC Standard No. 209-3B]

### 9.3.6 ***Auto Precharge Operation***

Before a new row in an active bank can be opened, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or a WRITE command is given to the device, the AP bit (CA0f) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst sequence.

If AP is HIGH when the READ or WRITE command is issued, then the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency) thus improving system performance for random data access.

#### ***Burst Read with Auto Precharge***

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto-precharge function is engaged. LPDDR3 devices start an auto-precharge operation on the rising edge of the clock BL/2 or BL/2 – 4 + RU( $t_{RTP}/t_{CK}$ ) clock cycles later than the READ with AP command, whichever is greater. For LPDDR3 auto-precharge calculations see Table 4. Following an auto-precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:

The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto-precharge begins.  
The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

[See Figure 24 in JEDEC Standard No. 209-3B]

#### ***Burst Write with Auto Precharge***

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge on the rising edge  $t_{WR}$  cycles after the completion of the burst WRITE.

Following a WRITE with auto precharge, an ACTIVATE command may be issued to the same bank if the following two conditions are met.

The RAS precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the auto-precharge begins.  
The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.

[See Figure 25 in JEDEC Standard No. 209-3B]

The minimum delays from the read, write and precharge commands to the various commands are summarized below.

**Table 4: Precharge & Auto Precharge clarification**

From Command	To Command	Minimum delay between "From Command" to "To Command"	Units	Notes
Read	Precharge (same bank)	$BL/2 + \text{Max}(4, RU(t_{RTP}/t_{CK})) - 4$	$t_{CK}$	1
	Precharge all	$BL/2 + \text{Max}(4, RU(t_{RTP}/t_{CK})) - 4$	$t_{CK}$	1
Read w/ AP	Precharge (same bank)	$BL/2 + \text{Max}(4, RU(t_{RTP}/t_{CK})) - 4$	$t_{CK}$	1,2
	Precharge all	$BL/2 + \text{Max}(4, RU(t_{RTP}/t_{CK})) - 4$	$t_{CK}$	1
	Activate (same bank)	$BL/2 + \text{Max}(4, RU(t_{RTP}/t_{CK})) - 4 + RU(t_{RPdb}/t_{CK})$	$t_{CK}$	1
	Write or Write w/ AP (same bank)	illegal	$t_{CK}$	3
	Write or Write w/ AP (different bank)	$RL + BL/2 + RU(t_{DQCKmax}/t_{CK}) - WL + 1$	$t_{CK}$	3
	Read or Read w/ AP (same bank)	illegal	$t_{CK}$	3
	Read or Read w/ AP (different bank)	$BL/2$	$t_{CK}$	3
Write	Precharge (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	$t_{CK}$	1
	Precharge all	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	$t_{CK}$	1
Write w/ AP	Precharge (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	$t_{CK}$	1
	Precharge all	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1$	$t_{CK}$	1
	Activate (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPdb}/t_{CK})$	$t_{CK}$	1
	Write or Write w/ AP (same bank)	illegal	$t_{CK}$	3
	Write or Write w/ AP (different bank)	$BL/2$		3
	Read or Read w/ AP (same bank)	illegal		3
	Read or Read w/ AP (different bank)	$WL + BL/2 + RU(t_{WTR}/t_{CK}) + 1$	$t_{CK}$	3
Precharge	Precharge (same bank)	1	$t_{CK}$	1
	Precharge all	1	$t_{CK}$	1
Precharge All	Precharge	1	$t_{CK}$	1
	Precharge all	1	$t_{CK}$	1

Notes:

- For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after  $t_{RP}$  depending on the latest precharge command issued to that bank.
- Any command issued during the minimum delay time as specified in Table 4 is illegal.
- After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read and Write operations may not be truncated or interrupted.

### 9.3.7 Refresh Command [REF]

The Refresh command is initiated by having CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per-bank REFRESH is initiated with CA3 LOW at the rising edge of the clock. All-bank REFRESH is initiated with CA3 HIGH at the rising edge of the clock.

A per-bank REFRESH command (REFpb) performs a per-bank REFRESH operation to the bank scheduled by the bank counter in the memory device. The bank sequence for per-bank REFRESH is fixed to be a sequential round-robin: 0-1-2-3-4-5-6-7-0-1-... The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET signal or at every exit from self refresh. Bank addressing for the per-bank REFRESH count is the same as established for the single-bank PRECHARGE command. A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met (see Table 5):

$t_{RFCab}$  has been satisfied after the prior REFab command

$t_{RFCpb}$  has been satisfied after the prior REFpb command

$t_{RP}$  has been satisfied after the prior PRECHARGE command to that bank

$t_{RRD}$  has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time ( $t_{RFCpb}$ ), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met (see Table 5):

$t_{RFCpb}$  must be satisfied before issuing a REFab command

$t_{RFCpb}$  must be satisfied before issuing an ACTIVATE command to the same bank

$t_{RRD}$  must be satisfied before issuing an ACTIVATE command to a different bank

$t_{RFCpb}$  must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met (see Table 5):

$t_{RFCab}$  has been satisfied following the prior REFab command

$t_{RFCpb}$  has been satisfied following the prior REFpb command

$t_{RP}$  has been satisfied following the prior PRECHARGE commands

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

$t_{RFCab}$  latency must be satisfied before issuing an ACTIVATE command

$t_{RFCpb}$  latency must be satisfied before issuing a REFab or REFpb command

**Table 5: REFRESH Command Scheduling Separation Requirements**

Symbol	From Command	To Command	Notes
$t_{RFCab}$	REFab	REFab	
		ACTIVATE command to any bank	
		REFpb	
$t_{RFCpb}$	REFpb	REFab	
		ACTIVATE command to same bank	
		REFpb	
$t_{RRD}$	REFpb	ACTIVATE command to different bank	1
	ACTIVATE	REFpb	
		ACTIVATE command to different bank	

Notes:

1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.

In general, an all bank refresh command needs to be issued to the LPDDR3 SDRAM regularly every  $t_{REFI}$  interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times t_{REFI}$  (see Figure 26). A maximum of 8 additional Refresh commands can be issued in advance (pulled in”), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times t_{REFI}$ . At any given time, a maximum of 16 REF commands can be issued within  $2 \times t_{REFI}$ .

And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of  $2 \times 8 \times 8$  per bank refresh commands can be issued within  $2 \times t_{REFI}$ .

[See Figures 26 - 28 in JEDEC Standard No. 209-3B]



### 9.3.8 ***Self-Refresh [SELF]***

The Self Refresh command can be used to retain data in the LPDDR3 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the SDRAM retains data without external clocking. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as  $t_{CPDED}$ . CKE LOW will result in deactivation of input receivers after  $t_{CPDED}$  has expired. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR3 SDRAM devices can operate in Self Refresh in both the standard or elevated temperature ranges. LPDDR3 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher at high temperatures.

Once the SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins ( $V_{DD1}$  and  $V_{DD2}$ ) must be at valid levels.  $V_{DDQ}$  may be turned off during Self-Refresh. Prior to exiting Self-Refresh,  $V_{DDQ}$  must be within specified limits.  $V_{refDQ}$  and  $V_{refCA}$  may be at any level within minimum and maximum levels (see Absolute Maximum DC Ratings). However prior to exiting Self- Refresh,  $V_{refDQ}$  and  $V_{refCA}$  must be within specified limits (see Recommended DC Operating Conditions). The SDRAM initiates a minimum of one all-bank refresh command internally within  $t_{CKESR}$  period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the SDRAM must remain in Self Refresh mode is  $t_{CKESR,min}$ . The user may change the external clock frequency or halt the external clock  $t_{CPDED}$  after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock shall be stable and within specified limits for a minimum of 2  $t_{CK}$  prior to the positive clock edge that registers CKE HIGH. Once Self Refresh Exit is registered, a delay of at least  $t_{XSR}$  must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period  $t_{XSR}$  for proper operation. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval  $t_{XSR}$ . For the description of ODT operation and specifications during self-refresh entry and exit, see section 9.3.16.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one REFRESH command (1 all-bank) is issued before entry into a subsequent Self Refresh.

[See Figure 31 in JEDEC Standard No. 209-3B]

Notes:

1. Input clock frequency may be changed or can be stopped or floated during self-refresh, provided that upon exiting self-refresh, the clock is stable and within specified limits for a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3.  $t_{XSR}$  begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after  $t_{XSR}$  is satisfied. NOPS shall be issued during  $t_{XSR}$ .

### 9.3.9 ***Mode Register Read Command***

The Mode Register Read (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f - CA0f and CA9r - CA4r. The mode register contents are available on the first data beat of DQ[7:0] after  $RL \times t_{CK} + t_{DQSQ} + t_{DQSQ}$  following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in the DQ Calibration specification. All DQS are toggled for the duration of the mode register read burst. The MRR command has a burst length of eight. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted.

[See Figure 32 in JEDEC Standard No. 209-3B]

Notes:

1. MRRs to DQ calibration registers MR32 and MR40 are described in DQ calibration section.
2. Only the NOP command is supported during  $t_{MRR}$ .
3. Mode register data is valid only on DQ[7:0] on the first beat. Subsequent beats contain valid but undefined data. DQ[MAX:8] contain valid but undefined data for the duration of the MRR burst.
4. Minimum Mode Register Read to write latency is  $RL + RU(t_{DQSQmax}/t_{CK}) + 8/2 + 1 - WL$  clock cycles.
5. Minimum Mode Register Read to Mode Register Write latency is  $RL + RU(t_{DQSQmax}/t_{CK}) + 8/2 + 1$  clock cycles.
6. In this example,  $RL = 8$  for illustration purposes only.

[See Figure 33 in JEDEC Standard No. 209-3B]

Notes:

1. Only the NOP command is supported during  $t_{MRR}$ .
2. The minimum number of clock cycles from the burst READ command to the MRR command is  $BL/2$ .

After a prior READ command, the MRR command must not be issued earlier than  $BL/2$  clock cycles, or  $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$  clock cycles after a prior WRITE command, as READ bursts and WRITE bursts must not be truncated by MRR.

[See Figure 34 in JEDEC Standard No. 209-3B]

Notes:

1. The minimum number of clock cycles from the burst WRITE command to the MRR command is  $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$ .
2. Only the NOP command is supported during  $t_{MRR}$ .

#### ***MRR Following Idle Power-Down State***

Following the idle power-down state, an additional time,  $t_{MRRi}$ , is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to  $t_{RCd}$ ) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from standby, idle power-down mode.

[See Figure 35 in JEDEC Standard No. 209-3B]

### 9.3.10 ***Mode Register Write Command***

The Mode Register Write (MRW) command is used to write configuration data to mode registers. The MRW (MRW) command is initiated by having CS<sub>n</sub> LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f - CA0f, CA9r - CA4r. The data to be written to the mode register is contained in CA9f – CA2f. The MRW command period is defined by  $t_{MRW}$ . Mode register WRITES to read-only registers have no impact on the functionality of the device.

[See Figure 38 in JEDEC Standard No. 209-3B]

The MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE-ALL command.

#### ***ZQ Calibration***

[See Section 4.11.2 in JEDEC Standard No. 209-3B]

### ***WR Leveling Mode***

In order to provide for improved signal integrity performance, the LPDDR3 SDRAM provides a write leveling feature to compensate for timing skew, affecting timing parameters such as  $t_{DQSS}$ ,  $t_{DSS}$ , and  $t_{DSH}$ .

The memory controller uses the write leveling feature to receive feedback from the SDRAM allowing it to adjust the clock to data strobe signal relationship for each DQS<sub>t</sub>/DQS<sub>c</sub> signal pair. The memory controller performing the leveling must have adjustable delay setting on DQS<sub>t</sub>/DQS<sub>c</sub> signal pair to align the rising edge of DQS signals with that of the clock signal at the DRAM pin. The DRAM asynchronously feeds back CLK, sampled with the rising edge of DQS signals. The controller repeatedly delays DQS signals until a transition from 0 to 1 is detected. The DQS signals delay established through this exercise ensures the tDQSS specification can be met.

All DQS signals may have to be leveled independently. During Write Leveling operations each DQS signal latches the clock with a rising strobe edge and drives the result on all DQ[n] of its respective byte.

The LPDDR3 SDRAM enters into write leveling mode when mode register MR2[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only NOP commands are allowed, or MRW command to exit write leveling operation. Upon completion of the write leveling operation, the DRAM exits from write leveling mode when MR2[7] is reset LOW.

The controller will drive DQS<sub>t</sub> LOW and DQS<sub>c</sub> HIGH after a delay of  $t_{WLDQSEN}$ . After time  $t_{WLMRD}$ , the controller provides DQS signal input which is used by the DRAM to sample the clock signal driven from the controller. The delay time  $t_{WLMRD(max)}$  is controller dependent. The DRAM samples the clock input with the rising edge of DQS and provides asynchronous feedback on all the DQ bits after time  $t_{WLO}$ . The controller samples this information and either increment or decrement the DQS<sub>t</sub> and/or DQS<sub>c</sub> delay settings and launches the next DQS/DQS# pulse. The sample time and trigger time is controller dependent. Once the following DQS<sub>t</sub>/DQS<sub>c</sub> transition is sampled, the controller locks the strobe delay settings, and write leveling is achieved for the device. Figure 45 describes the timing for the write leveling operation.

[See Figure 45 in JEDEC Standard No. 209-3B]

### 9.3.11 ***Power-Down [PDEN]***

Power-down is entered synchronously when CKE is registered LOW and CS<sub>n</sub> is HIGH at the rising edge of clock. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as row activation, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 50 through Figure 61.

Entering power-down deactivates the input and output buffers, excluding CKE. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as  $t_{CPDED}$ . CKE LOW will result in deactivation of input receivers after  $t_{CPDED}$  has expired.

In power-down mode, CKE must be held LOW; all other input signals are “Don’t Care.” CKE LOW must be maintained until  $t_{CKE,min}$  is satisfied.  $V_{REFCA}$  must be maintained at a valid level during power-down.

$V_{DDQ}$  can be turned off during power-down. If  $V_{DDQ}$  is turned off,  $V_{REFDQ}$  must also be turned off. Prior to exiting power-down, both  $V_{DDQ}$  and  $V_{REFDQ}$  must be within their respective minimum/maximum operating ranges.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is exited when CKE is registered HIGH. The controller must drive CS<sub>n</sub> HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until  $t_{CKE,min}$  is satisfied. A valid, executable command can be applied with power-down exit latency  $t_{XP}$  after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

[See Figure 50 in JEDEC Standard No. 209-3B]

NOTE : Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

[See Figure 51 in JEDEC Standard No. 209-3B]

[See Figure 52 in JEDEC Standard No. 209-3B]

NOTE : The pattern shown can repeat over an extended period of time. With this pattern, all AC and DC timing and voltage specifications with temperature and voltage drift are ensured.

[See Figure 53 in JEDEC Standard No. 209-3B]

NOTE 1: CKE must be held HIGH until the end of the burst operation.

NOTE 2: CKE can be registered LOW at  $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + BL/2 + 1$  clock cycles after the clock on which the READ command is registered

[See Figure 54 in JEDEC Standard No. 209-3B]

Notes:

1. CKE must be held HIGH until the end of the burst operation.
2. CKE can be registered LOW at  $RL + RU(t_{DQSCK}/t_{CK}) + BL/2 + 1$  clock cycles after the clock on which the READ command is registered.
3.  $BL/2$  with  $t_{RTP} = 7.5ns$  and  $t_{RAS(MIN)}$  is satisfied.
4. internal PRECHARGE.

[See Figure 55 in JEDEC Standard No. 209-3B]

NOTE : CKE can be registered LOW at  $WL + 1 + BL/2 + RU(t_{WR}/t_{CK})$  clock cycles after the clock on which the WRITE command is registered.

[See Figure 56 in JEDEC Standard No. 209-3B]

NOTE 1: CKE can be registered LOW at  $WL + 1 + BL/2 + RU(t_{WR}/t_{CK}) + 1$  clock cycles after the WRITE command is registered.

NOTE 2: Start internal PRECHARGE.

[See Figure 57 in JEDEC Standard No. 209-3B]

NOTE : CKE can go LOW  $t_{IHCKE}$  after the clock on which the REFRESH command is registered.

[See Figure 58 in JEDEC Standard No. 209-3B]

NOTE : CKE can go LOW at  $t_{IHCKE}$  after the clock on which the ACTIVATE command is registered.

[See Figure 59 in JEDEC Standard No. 209-3B]

NOTE : CKE can go LOW  $t_{IHCKE}$  after the clock on which the PRECHARGE command is registered.

[See Figure 60 in JEDEC Standard No. 209-3B]

NOTE 1: CKE can be registered LOW  $RL + RU(t_{DQACK}/t_{CK}) + BL/2 + 1$  clock cycles after the clock on which the MRR command is registered.

NOTE 2: CKE should be held high until the end of the burst operation.

[See Figure 61 in JEDEC Standard No. 209-3B]

NOTE 1: CKE can be registered LOW  $t_{MRW}$  after the clock on which the MRW command is registered.

### 9.3.12 *Deep Power-Down [DPDEN]*

Deep Power-Down is entered when CKE is registered LOW with CS<sub>n</sub> LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW. The contents of the SDRAM will be lost upon entry into Deep Power-Down mode.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. To ensure that there is enough time to account for internal delay on the CKE signal path, two NOP commands are required after CKE is driven LOW, this timing period is defined as  $t_{CPDED}$ . CKE LOW will result in deactivation of command and address receivers after  $t_{CPDED}$  has expired. All power supplies must be within specified limits prior to exiting Deep Power-Down.  $V_{refDQ}$  and  $V_{refCA}$  may be at any level within minimum and maximum levels (see 4.1). However prior to exiting Deep Power-Down,  $V_{ref}$  must be within specified limits (See 4.3).

The Deep Power-Down state is exited when CKE is registered HIGH, while meeting  $t_{ISCKE}$  with a stable clock input. The SDRAM must be fully re-initialized as described in the power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence is completed. For the description of ODT operation and specifications during DPD entry and exit, see 9.3.16.

[See Figure 62 in JEDEC Standard No. 209-3B]

Notes:

1. Initialization sequence may start at any time after  $T_c$ .
2.  $t_{INIT3}$ , and  $T_c$  refer to timings in the LPDDR3 initialization sequence. For more detail, see 9.1.
3. Input clock frequency may be changed or the input clock can be stopped or floated during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

### 9.3.13 ***Input Clock Stop and Frequency Change***

LPDDR3 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab command may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.
- After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE LOW under the following conditions:

- CK\_t is held LOW and CK\_c is held HIGH or both are floated during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab command may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions ( $t_{RCD}$ ,  $t_{RP}$ ) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR3 devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{CK(ABS)min}$  is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to changing the frequency;
- CS\_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REFab command may be executing;
- The LPDDR3 SDRAM is ready for normal operation after the clock satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 * t_{CK} + t_{XP}$ .
- After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR3 devices support clock stop during CKE HIGH under the following conditions:

1. CK\_t is held LOW and CK\_c is held HIGH during clock stop;
2. CS\_n shall be held HIGH during clock stop;
3. Refresh requirements apply during clock stop;
4. During clock stop, only REFab command may be executing;
5. Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
6. The related timing conditions ( $t_{RCD}$ ,  $t_{WR}$ ,  $t_{WRA}$ ,  $t_{RP}$ ,  $t_{MRW}$ ,  $t_{MRR}$ , etc.) have been met prior to stopping the clock;
7. The LPDDR3 SDRAM is ready for normal operation after the clock is restarted and satisfies  $t_{CH(ABS)}$  and  $t_{CL(ABS)}$  for a minimum of  $2 * t_{CK} + t_{XP}$ .

### 9.3.14 ***No Operation Command [NOP]***

The purpose of the No Operation command (NOP) is to prevent the LPDDR3 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

CS\_n HIGH at the clock rising edge N (DESL).

CS\_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N (NOP).

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

**9.3.15 Temperature Sensor**

LPDDR3 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device  $T_{OPER}$  (see 4.2) may be used to determine whether operating temperature requirements are being met.

LPDDR3 devices shall monitor device temperature and update MR4 according to  $t_{TSI}$ . Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than  $t_{TSI}$ .

When using the temperature sensor, the actual device case temperature may be higher than the  $T_{OPER}$  specification (see 4.2) that applies for the standard or elevated temperature ranges. For example,  $T_{CASE}$  may be above 85°C when MR4[2:0] equals 'b011. LPDDR3 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller re-configures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors: TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval ( $t_{TSI}$ ) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + t_{TSI} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$

**Table 6: Temperature Sensor**

Parameter	Symbol	Max/Min	Value	Unit	Notes
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	$t_{TSI}$	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C/s	

For example, if TempGradient is 10°C/s and the SysRespDelay is 1 ms:

$$10^\circ\text{C/s} \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^\circ\text{C}$$

In this case, ReadInterval shall be no greater than 167 ms.

[See Figure 36 in JEDEC Standard No. 209-3B]



### 9.3.16 ***ODT***

ODT (On-Die Termination) is a feature of the LPDDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS<sub>t</sub>, DQS<sub>c</sub> and DM via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. Unlike other command inputs, the ODT pin directly controls ODT operation and is not sampled by the clock.

The ODT feature is turned off and not supported in Self-Refresh and Deep Power Down modes. ODT operation can optionally be enabled during CKE Power Down via a mode register. Note that if ODT is enabled during Power Down mode VDDQ may not be turned off during Power Down. The DRAM will also disable termination during read operations.

A simple functional representation of the DRAM ODT feature is shown in Figure 46.

[See Figure 46 in JEDEC Standard No. 209-3B]

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other mode register control information. The value of  $R_{TT}$  is determined by the settings of Mode Register bits. The ODT pin will be ignored if the Mode Register MR11 is programmed to disable ODT, in self-refresh, in deep power down, in CKE power down (mode register option) and during read operations.

#### ***ODT Mode Register***

The ODT Mode is enabled if MR11 OP<1:0> are non zero. In this case, the value of  $R_{TT}$  is determined by the settings of those bits. The ODT Mode is disabled if MR11 OP<1:0> are zero.

MR11 OP<2> determines whether ODT, if enabled through MR11 OP<1:0>, will operate during CKE power down.

#### ***Asynchronous ODT***

The ODT feature is controlled asynchronously based on the status of the ODT pin, except ODT is off when:

- ODT is disabled through MR11 OP<1:0>
- DRAM is performing a read operation (RD or MRR)
- DRAM is in CKE Power Down and MR11 OP<2> is zero
- DRAM is in Self-Refresh or Deep Power Down modes.
- DRAM is in CA Training Mode.

In asynchronous ODT mode, the following timing parameters apply when ODT operation is controlled by the ODT pin:

$t_{ODTon,min,max}$ ,  $t_{ODToff,min,max}$ .

Minimum  $R_{TT}$  turn-on time ( $t_{ODTon,min}$ ) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum  $R_{TT}$  turn on time ( $t_{ODTon,max}$ ) is the point in time when the ODT resistance is fully on.  $t_{ODTon,min}$  and  $t_{ODTon,max}$  are measured from ODT pin high.

Minimum  $R_{TT}$  turn-off time ( $t_{ODToff,min}$ ) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time ( $t_{ODToff,max}$ ) is the point in time when the on-die termination has reached high impedance.  $t_{ODToff,min}$  and  $t_{ODToff,max}$  are measured from ODT pin low.

#### ***ODT During Read Operations (RD or MRR)***

During read operations, LPDDR3 SDRAM will disable termination and disable ODT control through the ODT pin. After read operations are completed, ODT control is resumed through the ODT pin (if ODT Mode is enabled).

### ODT During Power Down

When MR11 OP<2> is zero, termination control through the ODT pin will be disabled when the DRAM enters CKE power down. After a power down command is registered, termination will be disabled within a time window specified by  $t_{ODTd,min,max}$ . After a power down exit command is registered, termination will be enabled within a time window specified by  $t_{ODTe,min,max}$ .

Minimum  $R_{TT}$  disable time ( $t_{ODTd,min}$ ) is the point in time when the device termination circuit will no longer be controlled by the ODT pin. Maximum ODT disable time ( $t_{ODTd,max}$ ) is the point in time when the on-die termination will be in high impedance.

Minimum  $R_{TT}$  enable time ( $t_{ODTe,min}$ ) is the point in time when the device termination circuit will no longer be in high impedance. The ODT pin shall control the device termination circuit after maximum ODT enable time ( $t_{ODTe,max}$ ) is satisfied.

When MR11 OP<2> is enabled and MR11 OP<1:0> are non zero, ODT operation is supported during CKE power down with ODT control through the ODT pin.

### ODT During Self Refresh

LPDDR3 SDRAM disables the ODT function during self refresh. After a self refresh command is registered, termination will be disabled within a time window specified by  $t_{ODTd,min,max}$ . After a self refresh exit command is registered, termination will be enabled within a time window specified by  $t_{ODTe,min,max}$ .

### ODT During Deep Power Down

LPDDR3 SDRAM disables the ODT function during deep power down. After a deep power down command is registered, termination will be disabled within a time window specified by  $t_{ODTd,min,max}$ .

### ODT During CA Training and Write Leveling

During CA Training Mode, LPDDR3 SDRAM will disable on-die termination and ignore the state of the ODT control pin. For ODT operation during Write Leveling mode, refer to Table 7 for termination activation and deactivation for DQ and DQS<sub>t</sub>/DQS<sub>c</sub>.

**Table 7: DRAM Termination Function In Write Leveling Mode**

ODT pin	DQS <sub>t</sub> /DQS <sub>c</sub> termination	DQ termination
de-asserted	OFF	OFF
asserted	ON	OFF

If ODT is enabled, the ODT pin must be high, in Write Leveling mode.

**Table 8: ODT States Truth Table**

	Write	Read/ DQ Cal	ZQ Cal	CA Training	Write Level
DQ Termination	Enabled	Disabled	Disabled	Disabled	Disabled
DQS Termination	Enabled	Disabled	Disabled	Disabled	Enabled

NOTE : ODT is enabled with MR11[1:0]='b01, 'b10, or 'b11 and ODT pin HIGH. ODT is disabled with MR11[1:0]='b00 or ODT pin LOW.

[See Figure 47 in JEDEC Standard No. 209-3B]

[See Figure 48 in JEDEC Standard No. 209-3B]

NOTE 1: The automatic  $R_{TT}$  turn-off delay,  $t_{AODToff}$ , is referenced from the rising edge of "RL-2" clock at  $T_{m-2}$ .

NOTE 2: The automatic  $R_{TT}$  turn-on delay,  $t_{AODTon}$ , is referenced from the rising edge of "RL+ BL/2" clock at  $T_{m+4}$ .

[See Figure 49 in JEDEC Standard No. 209-3B]

NOTE 1: Upon exit of Deep Power Down mode, a complete power-up initialization sequence is required.

Change History			
Rev. #	Who	When	What
0.1	HCLIN	2017-08-22	Initial Version
0.2	HCLIN	2017-09-19	Revised Block Diagram
0.3	HCLIN	2017-12-12	Removed tREFBW
0.4	JECY	2018-02-21	Added PoP216 package
0.5	LANCE	2018-06-05	modify interface information from LVCMOS to HSUL_12
0.6	LANCE	2018-07-06	modify temperature grade code of PN code from XT to X
0.7	LANCE	2018-08-02	1. modify idd spec 2. remove pop216, add bga134 of package information
0.8	Jerry	2019-05-27	Modified Idd spec. and ordering information
0.9	David	2019-10-08	The max CLK frequency is 933MHz for PKG only
1.0a	David	2019-11-08	134B -AB only under normal operation
1.0b	Jacky	2020-04-28	Modify bit[4] tested Die of MR9 to Reserved.
1.0c	Jacky	2021-09-07	1.Revised part number by BD suggestions to promote 2.by DV comment : revised Average refresh period: 7.8uS @ < 85°C, 1.95uS @ < 105°C 3.Remove X16 part number, do not promote
1.1	Ian	2021-12-23	Remove VDDCA & VSSCA description revised typo "inputsa" to "inputs" revised typo "requency" to "frequency"
1.2	Wayne/Lance	2022/8/16	1. table format modify 2. Revise naming rule table 3. remove x16 information 4. correct error description
1.3	Wayne	2023/09/26	Add note for Clock Frequency: 933(*)/800/667/533MHz(*: with VDD2 and VDDQ= 1.17 to 1.3V) Add VDD2 and VDDQ= 1.17 to 1.3V condition to Difference from JEDEC