SPI/QPI PSRAM

Specifications

- **Single Supply Voltage**
  - V_{DD}=1.62 to 1.98V
- **Interface**: SPI/QPI with SDR mode
- **Performance**: Clock rate up to
  - 144MHz for Wrapped Burst operation
  - 84MHz for Linear 2048 Burst operation
- **Organization**: 128Mb, 16M x 8bits
- **Addressable Bit Range**: A[23:0]
- **Page Size**: 2048 bytes
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - Tc= -40°C to +85°C (standard range)
  - Tc= -40°C to +105°C (extended range)
- **Maximum Standby Current**
  - 590µA @ 105°C
  - 420µA @ 85°C
- **Typical HalfSleep™ Mode with data retained**
  - 19.5µA @ 25°C

Features

- **Output Driver LVCMOS** with programmable drive strengths of 50, 100 and 200Ω
- **Dedicated Wrapped Burst** read and write commands
- **Linear 2048 Length Burst** is supported up to 84MHz and can cross page boundary as long as tCEM is met
- **Register Configurable Wrap Lengths** of 16, 32, 64 and 2048
- **Software Reset**

Table of Contents

1 Table of Contents

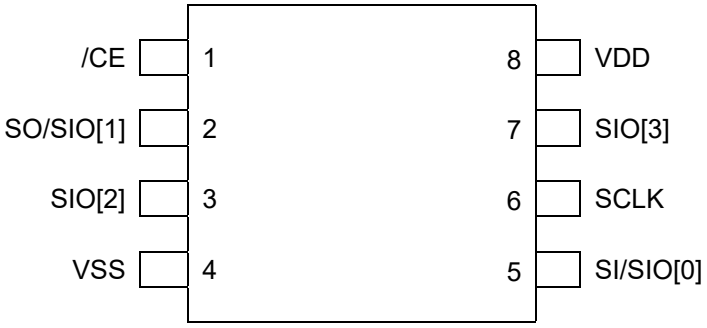
2 Introduction

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 I/O pins and operates in SPI(serial peripheral interface) or QPI (quad peripheral interface) mode with frequencies up to 144 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

3 Package Information

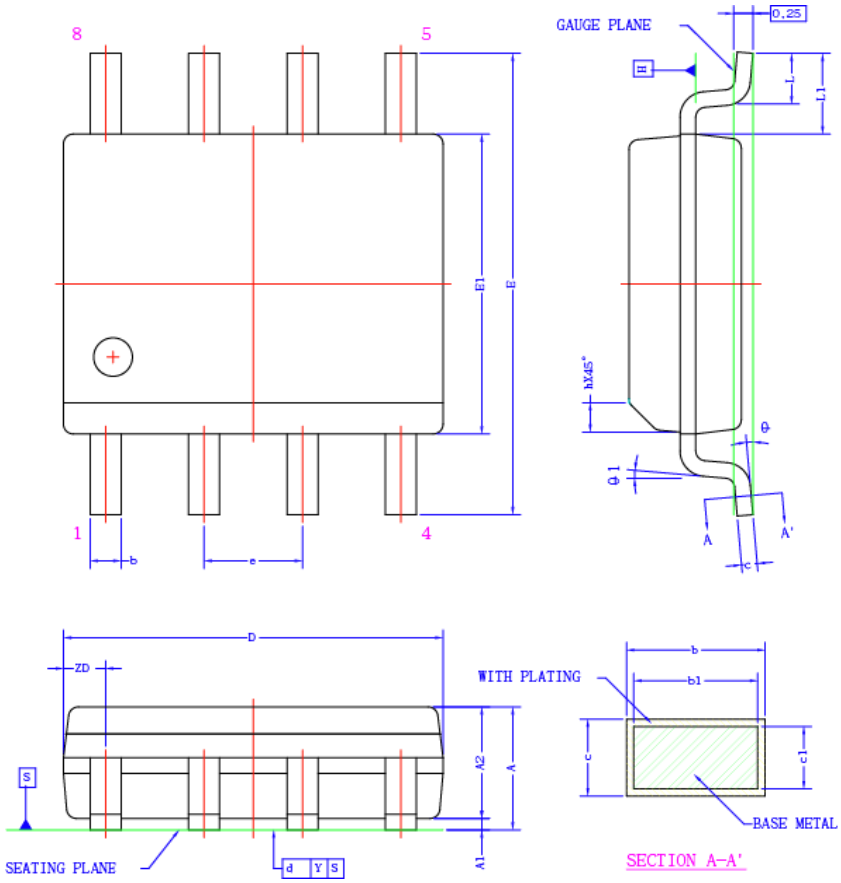
The APS12804O-SQRH is available in 8-lead SOP-8L(150).

3.1 Package Types : SOP (SN) , not to scale, Top view



4 Package Outline Drawing

4.1 SOP-8L(150), package code SN



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2	1.35	1.45	1.55	53	57	61
b	0.31	–	0.51	12	–	20
b1	0.28	0.40	0.48	11	16	19
c	0.17	–	0.25	7	–	10
c1	0.17	0.20	0.23	7	8	9
D	4.80	4.90	5.00	189	193	197
E	6.00 BSC			236 BSC		
E1	3.80	3.90	4.00	150	154	157
e	1.27 BSC			50 BSC		
L	0.40	0.66	1.27	16	26	50
L1	1.05 REF			41 REF		
ZD	0.55 REF			22 REF		
h	0.25	0.38	0.50	10	15	20
Y	–	–	0.10	–	–	4
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–

NOTE :

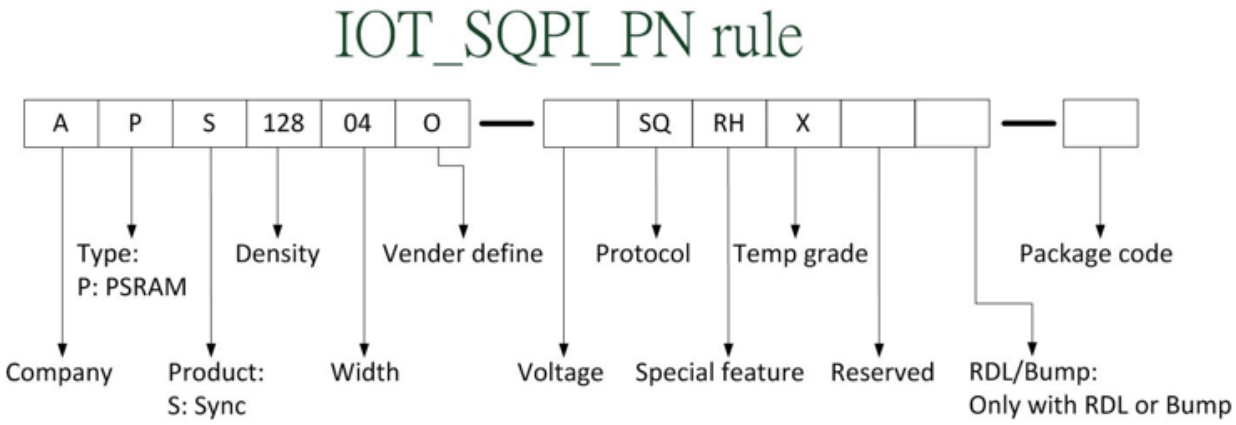
1. REFER TO JEDEC STD: MS-012 AA.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION "E1" DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
   'D' AND 'E1' DIMENSIONS ARE DETERMIND AT DATUM H .
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

5 Ordering Information

Table 1: Ordering Information

Part Number	*IO*	*Temperature Range*	*Max Frequency*	*Note*
APS12804O-SQRH	X4	Tj=-40°C to +85°C	144 MHz*	Bare die, SIP
APS12804O-SQRHX	X4	Tj=-40°C to +105°C	144 MHz*	Bare die, SIP
APS12804O-SQRH-SN	X4	Tc=-40°C to +85°C	144 MHz*	SOP8 (Only for validation)

Note *: 144MHz for Wrapped Burst operation
84MHz for Linear 2048 Burst operation with RBX(row boundary crossing)



6 Signal Table

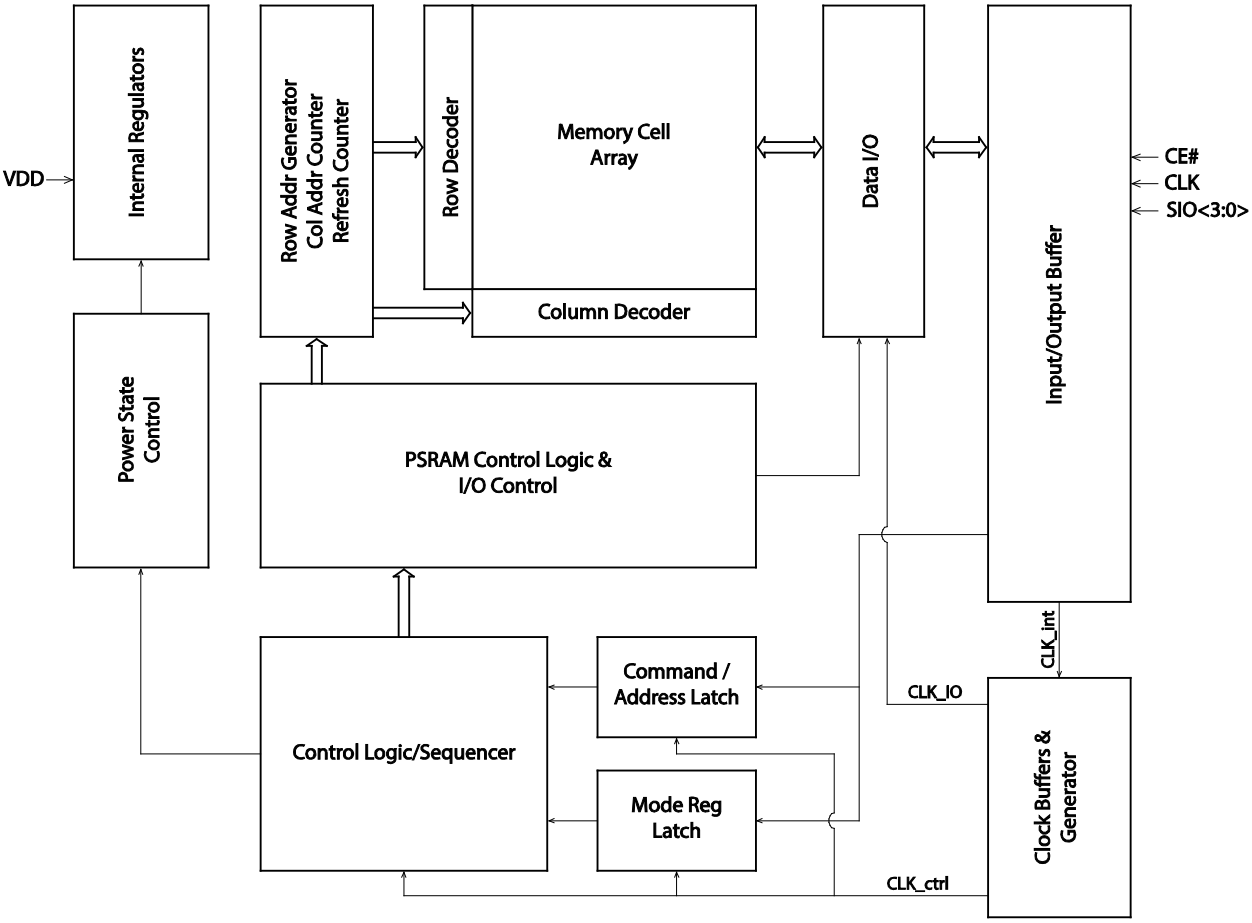
All signals are listed in Table 2.

Table 2: Signals Table

Symbol	*Type*	*SPI Mode Function*		*QPI Mode Function*	*Comments*
VDD	Power	Core supply 1.8V			
VSS	Ground	Core supply ground			
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state			
CLK	Input	Clock Signal			
SI/SIO[0]	IO	Serial Input	IO[0]*	IO[0]	
SO/SIO[1]	IO	Serial Output	IO[1]*	IO[1]	
SIO[2]	IO	--	IO[2]*	IO[2]	
SIO[3]	IO	--	IO[3]*	IO[3]	

Note *: SPI Quad mode

7 Block Diagram



8 Power-Up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{DD} reaches a stable level at or above minimum V_{DD}, the device will require 150µs and user-issued RESET Operation (see section 17) to complete its self-initialization process. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track V_{DD} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

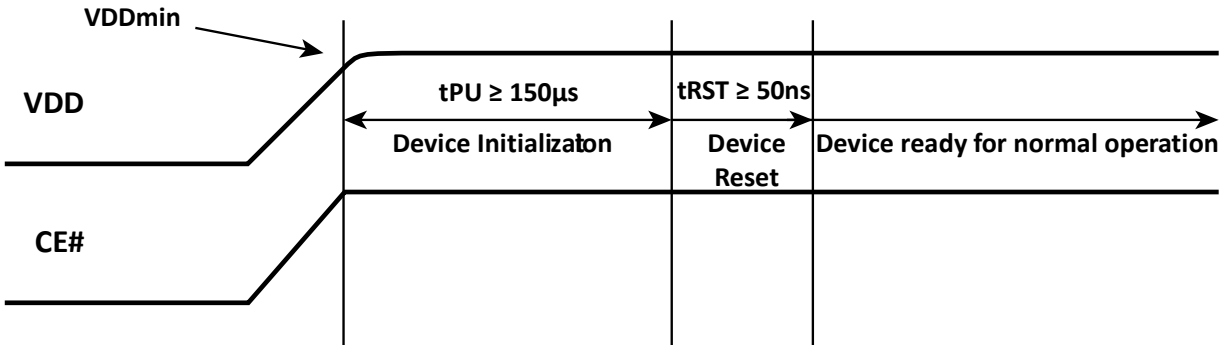


Figure 1. Power-Up Initialization Timing

9 Interface Description

9.1 Address Space

SPI/QPI PSRAM device is byte-addressable. 128M device is addressed with A[23:0].

9.2 Page Length

Read and write operations are default page size of 2048 bytes.

9.3 Drive Strength

The device powers up in 50Ω.

9.4 Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

10 Mode Register Definition

Table 3: Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h0	R/W	rsvd.	Wrap		rsvd.			DQ Zout	

Table 4: Wrap Codes MR0[6:5]

Wrap Burst Settings		Page Boundary Crossing	
MR0[6:5]	Wrapped Length	Non-Wrap CMDs ('h03,'h0B,`hEB,'h02,'h38)	Wrap CMDs('h8B,'h82)
00	16	Wrap 16, no cross page boundary	
01	32	Wrap 32, no cross page boundary	
10	64	Wrap 64, no cross page boundary	
11 (default)	2048 (page size)	Linear, can cross page boundary	Wrap 2048, no cross page boundary

Table 5: DQ Output Drive Strength Codes MR0[1:0]

DQ Output Drive Strength	
MR0[1:0]	Impedance
00(default)	50Ω
01	100Ω
10	200Ω
others	reserved

11 Command/Address Latching Truth Table

		SPI Mode (QE=0)					QPI Mode (QE=1)				
Command	**Code**	**Cmd**	**Addr**	**Wait Cycle**	**DIO**	**Max Freq.**	**Cmd**	**Addr**	**Wait Cycle**	**DIO**	**Max Freq.**
Read	'h03	S	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	144/84*	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	144/84*	Q	Q	6	Q	144/84*
Write	'h02	S	S	0	S	144/84*	Q	Q	0	Q	144/84*
Quad Write	'h38	S	Q	0	Q	144/84*	same as 'h02				
Wrapped Read	h8B	S	S	8	S	144	Q	Q	6	Q	144
Wrapped Write	h82	S	S	0	S	144	Q	Q	0	Q	144
Mode Register Read	hB5	S	S	8	S	144	Q	Q	6	Q	144
Mode Register Write	hB1	S	S	0	S	144	Q	Q	0	Q	144
Enter Quad Mode	'h35	S	-	-	-	144	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	144
Reset Enable	'h66	S	-	-	-	144	Q	-	-	-	144
Reset	'h99	S	-	-	-	144	Q	-	-	-	144
Half Sleep Entry	'hC0	S	-	-	-	144	Q	-	-	-	144
Read ID	'h9F	S	S	0	S	33	N/A				

Remark: S = Serial IO, Q = Quad IO

The device recognizes the following commands specified by the various input methods.

Note *: Linear 2048 Length burst can be performed *crossing page boundary(RBX)* by non-Wrapped burst commands issued while setting of MR0[6:5]=11. Frequency limits are therefore: *Max Freq.* is up to 84MHz when *Linear 2048 Length,* and *Max Freq.* is 144MHz under Wrapped Burst Operation.

11.1 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

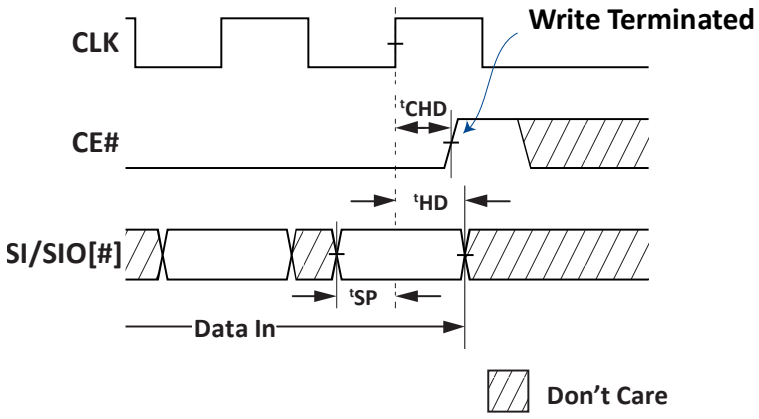


Figure 2: Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (^{t}CHD > ^{t}ACLK+^{t}CLK) for a sufficient data window.

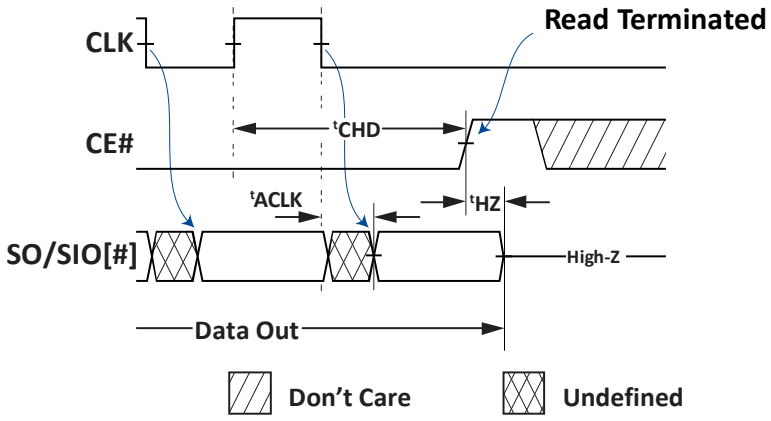


Figure 3: Read Command Termination

12 Mode Register Operations

12.1 SPI MR Read Operation

For all reads, MR data will be available ^{t}ACLK after the falling edge of CLK.

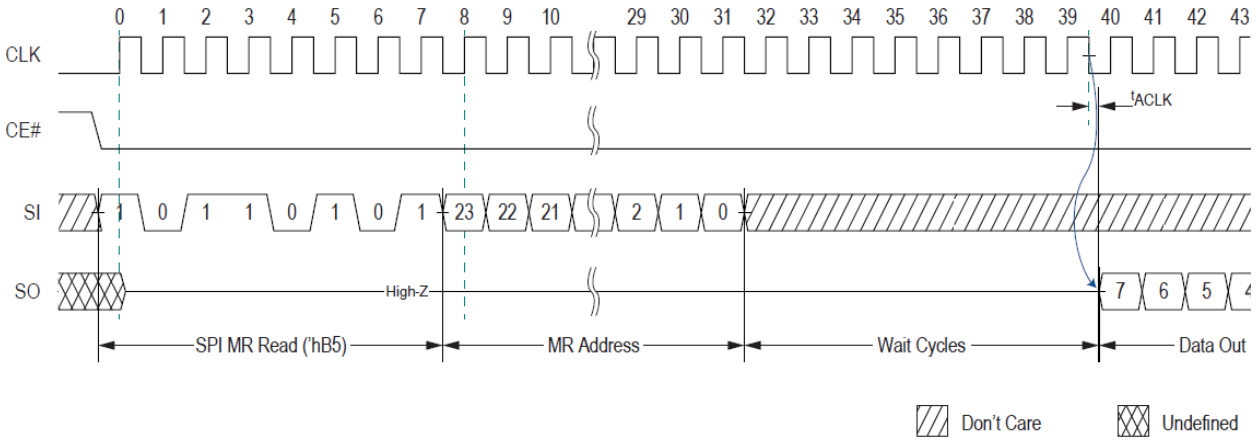


Figure 4: SPI MR Read 'hB5

12.2 SPI MR Write Operation

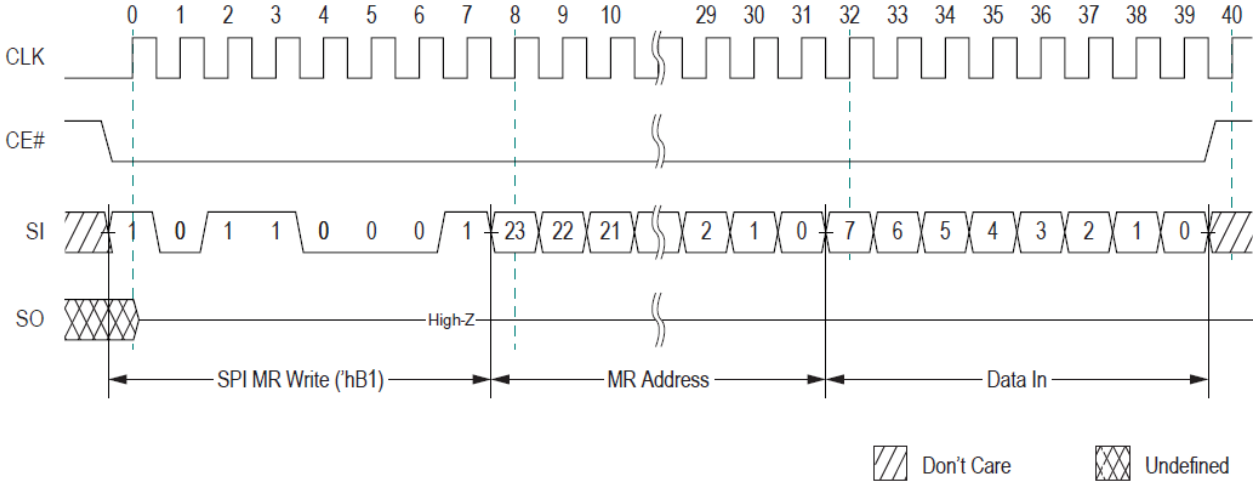


Figure 5: SPI MR Write 'hB1

12.3 QPI MR Read Operation

For all reads, MR data will be available ^{t}ACLK after the falling edge of CLK.

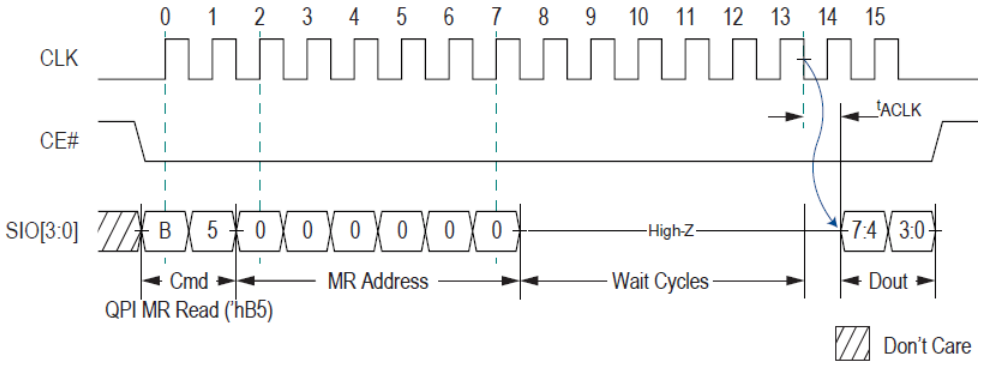


Figure 6: QPI MR Read 'hB5

12.4 QPI MR Write Operation

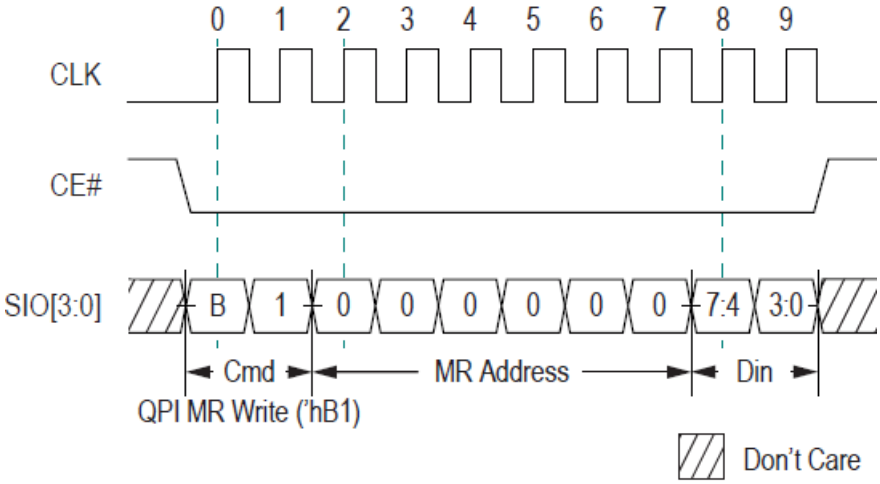


Figure 7: QPI MR Write 'hB1

13 Read ID

Read ID command provides information of vendor ID, known-good-die, device density, and manufacturing ID. Note that Read ID command can be used ONLY as Power up initialization after the device Reset tRST≧ 50ns right after Global Reset command.

Figure 8: Pre-condition of EID Read

13.1 SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

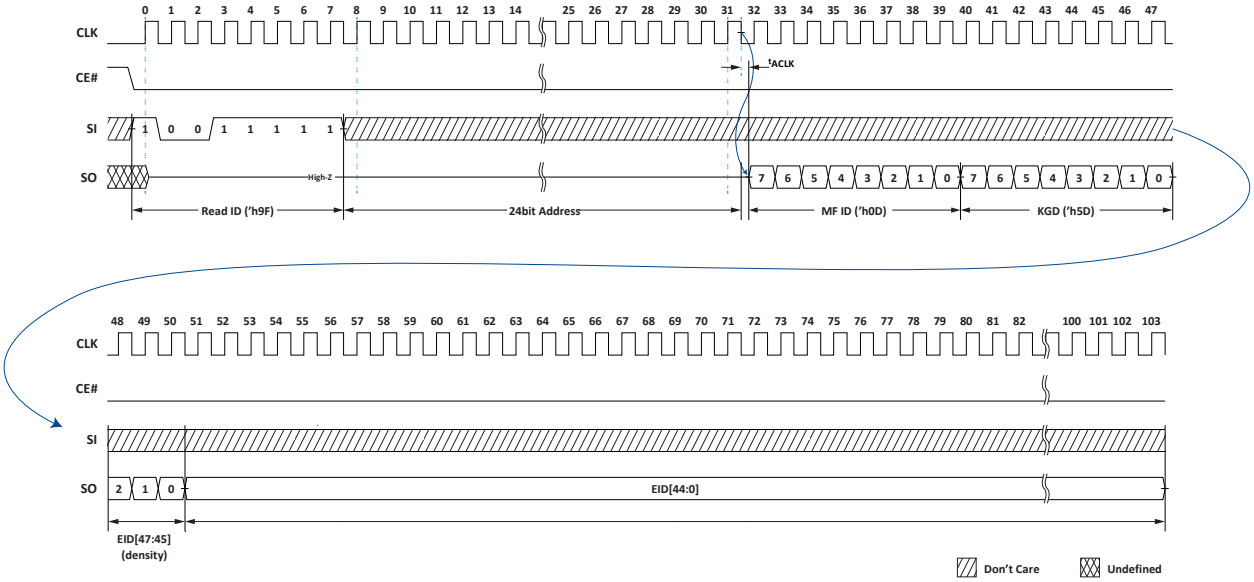


Figure 9: SPI Read ID 'h9F (available only in SPI mode)

14 Halfsleep™ mode Operation

Halfsleep™ Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry can be entered by issuing a command 'hC0. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of ^{t}HS. The Halfsleep™ Entry command sequences are shown below.

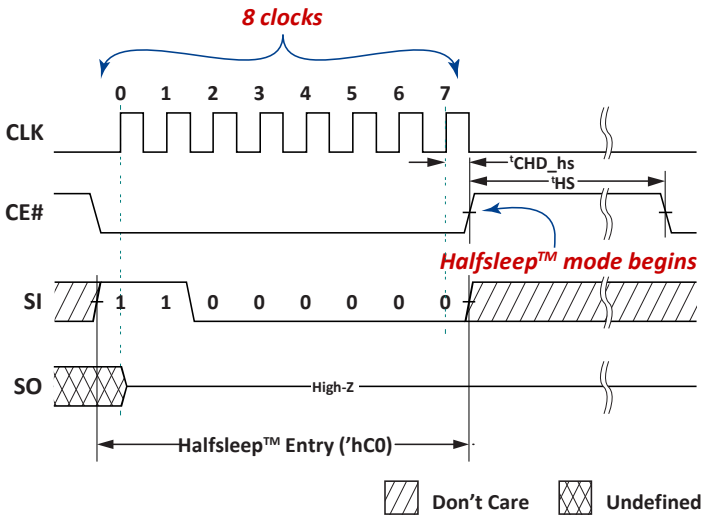


Figure 10: SPI Halfsleep™ Entry 'hC0.

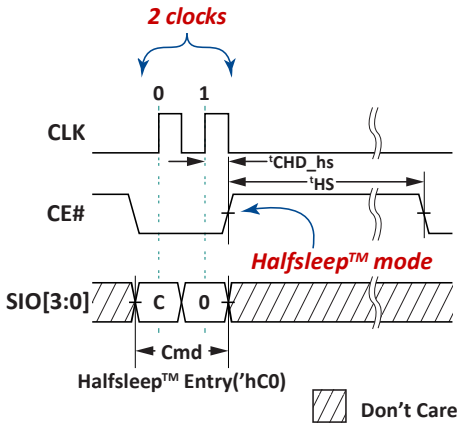


Figure 11: QPI Halfsleep™ Entry 'hC0.

Halfsleep™ Exit is inited by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

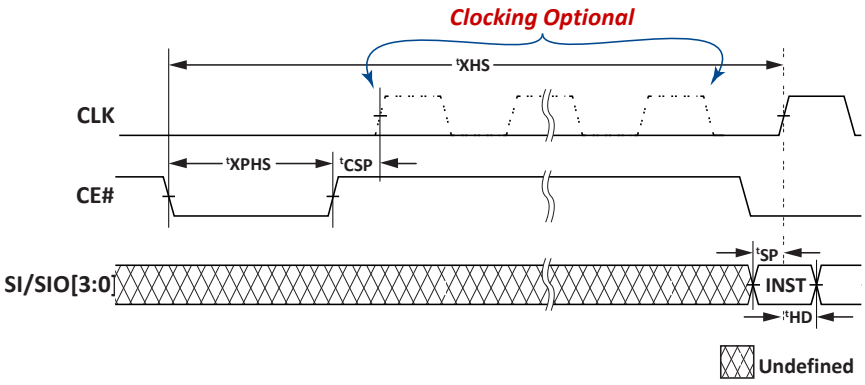


Figure 12: Halfsleep™ Exit

15 SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

15.1 SPI Read Operations

For all reads, data will be available ^{t}ACLK after the falling edge of CLK.

SPI Reads can be done in four ways:

1. ‘h03: Serial CMD, Serial Addr/IO, slow frequency, with wrap or linear bursting.
2. ‘h0B: Serial CMD, Serial Addr/IO, fast frequency, with wrap or linear bursting.
3. ‘hEB: Serial CMD, Quad Addr/IO, fast frequency, with wrap or linear bursting.
4. ‘h8B: Serial CMD, Serial Addr/IO, fast frequency, with forced wrap (register configurable lengths).

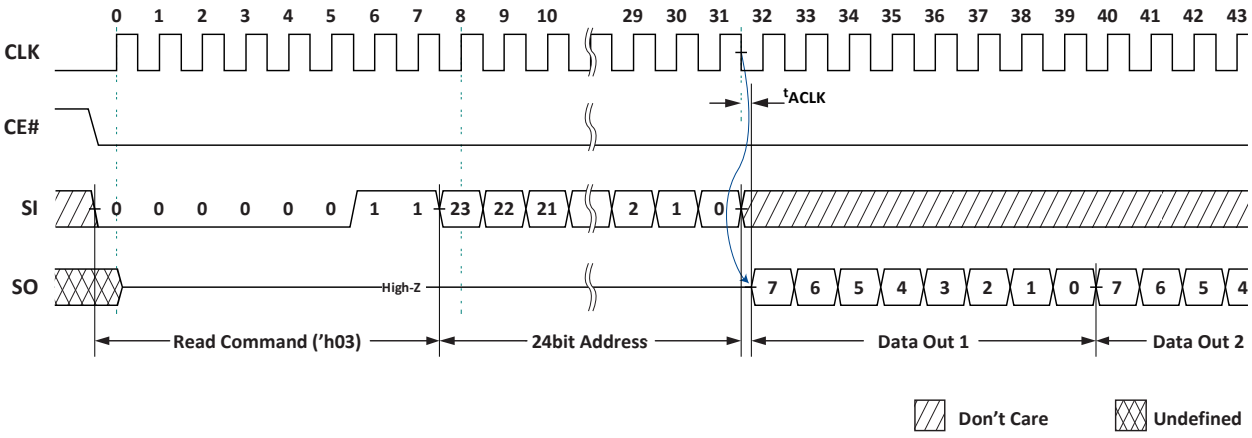


Figure 13: SPI Read ‘h03 (max freq 33MHz)

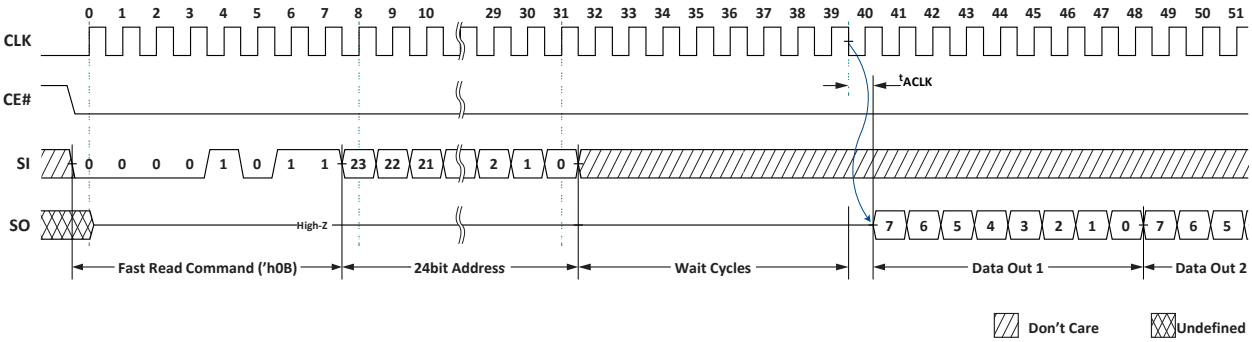


Figure 14: SPI Fast Read ‘h0B (max freq 144/84 MHz)

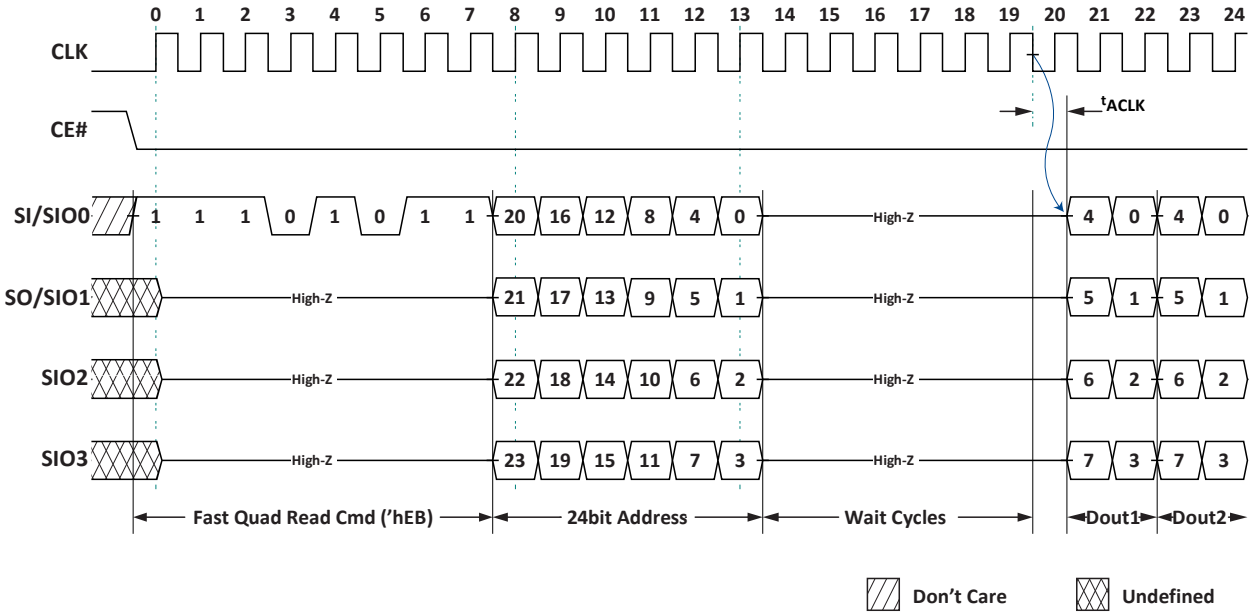


Figure 15: SPI Fast Quad Read 'hEB (max freq 144/84 MHz)

15.2 SPI Write Operations

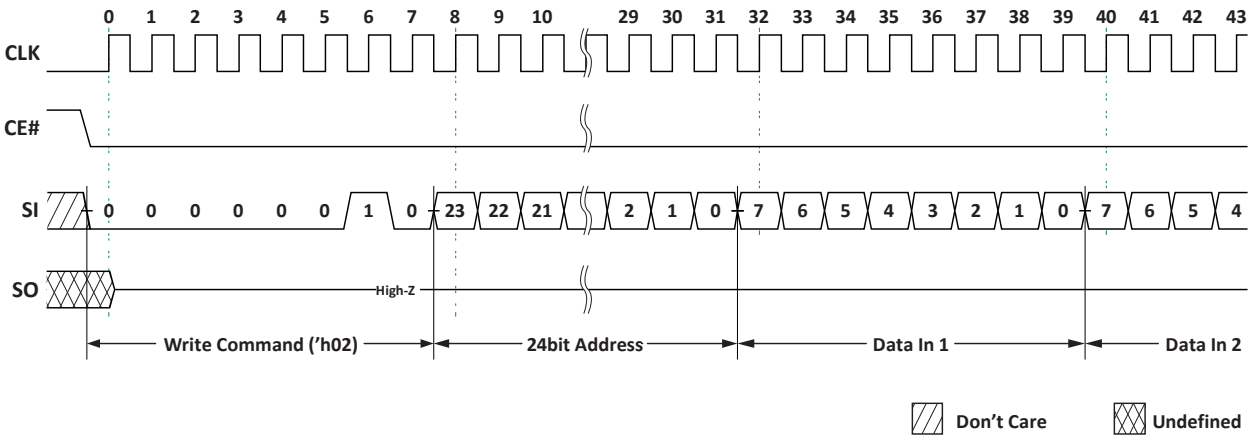


Figure 16: SPI Write 'h02

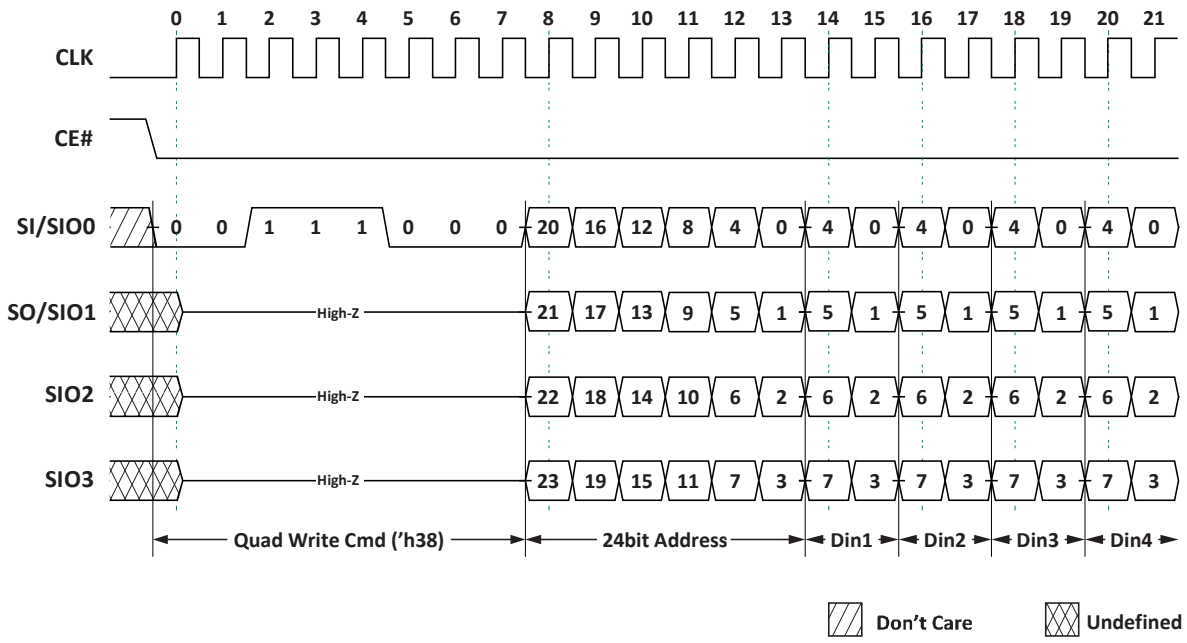


Figure 17: SPI Quad Write 'h38

15.3 SPI Quad Mode Enable Operation

This command switches the device into quad IO mode.

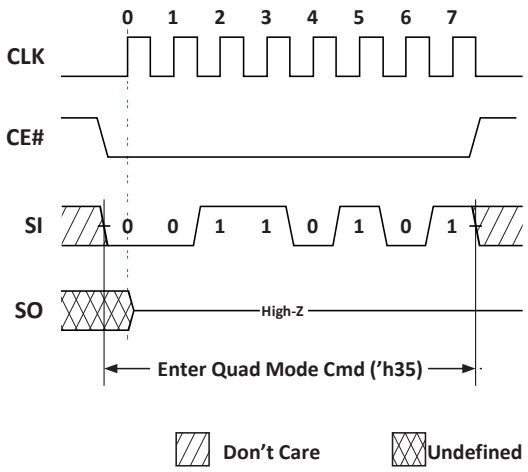


Figure 18: Quad Mode Enable ‘h35 (available only in SPI mode)

16 QPI Mode Operations

16.1 QPI Read Operations

For all reads, data will be available ^{t}ACLK after the falling edge of CLK.

QPI Reads can be done in one of three ways:

1. ‘h0B: Quad CMD, Addr & IO, slow frequency with wrap or linear bursting.
2. ‘hEB: Quad CMD, Addr & IO, fast frequency with wrap or linear bursting.
3. ‘h8B: Quad CMD, Addr & IO, fast frequency with forced wrap (register configurable lengths).

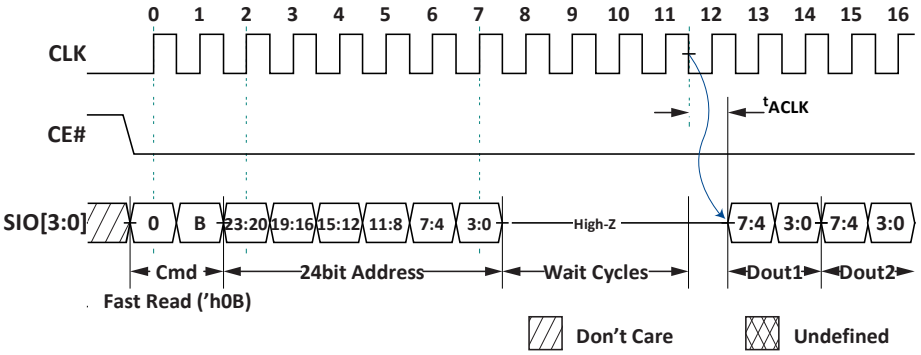


Figure 19: QPI Fast Read ‘h0B (max freq 66 MHz)

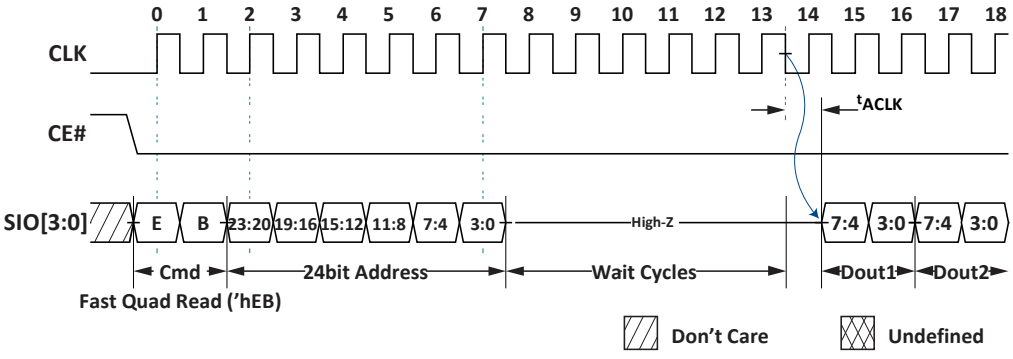


Figure 20: QPI Fast Quad Read ‘hEB (max freq 144/84 MHz)

16.2 QPI Write Operation(s)

QPI write command can be done in one of two ways:

1. ‘h02 or ‘h38: Quad CMD, Addr & IO, with wrap or linear bursting.
2. ‘h82: Quad CMD, Addr & IO, with forced wrap (register configurable lengths).

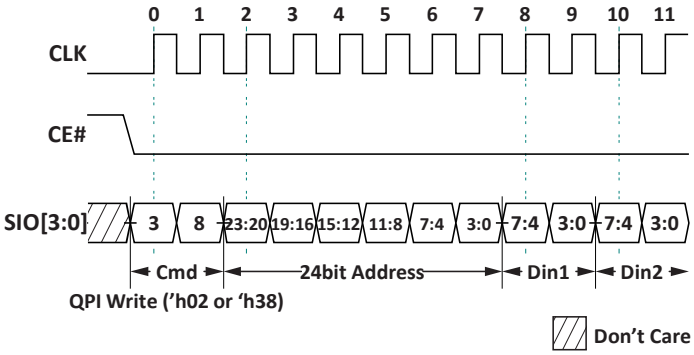


Figure 21: QPI Write

16.3 QPI Quad Mode Exit operation

This command will switch the device back into serial IO mode.

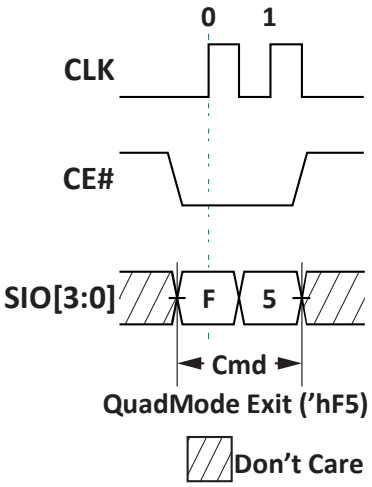


Figure 22: Quad Mode Exit ‘hF5 (only available in QPI mode)

17 Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

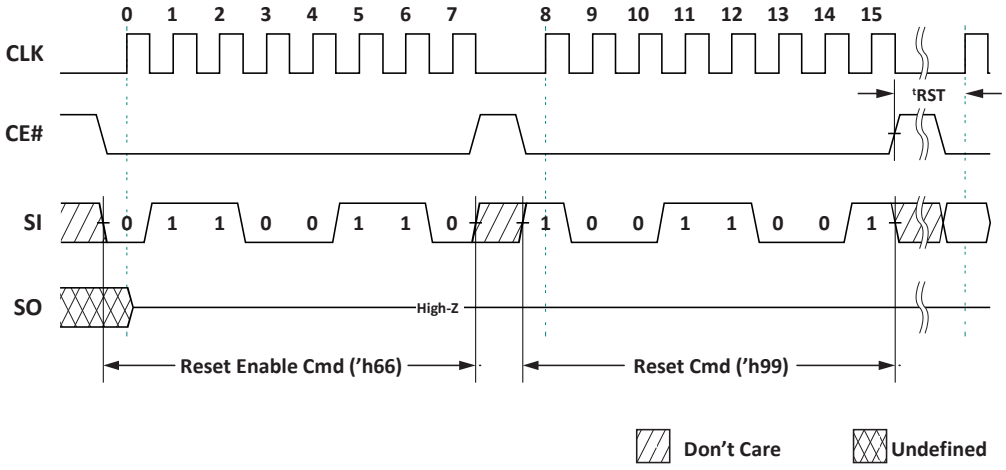


Figure 23: SPI Reset

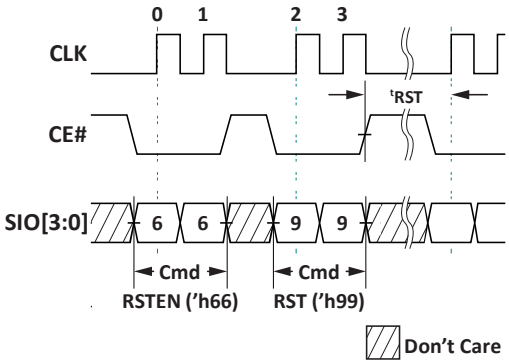


Figure 24: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

18 Input/Output Timing

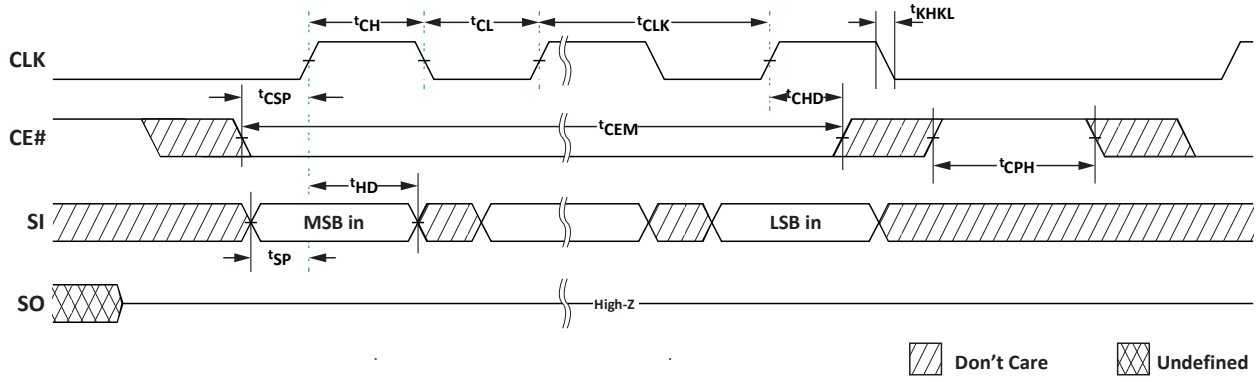


Figure 25: Input Timing

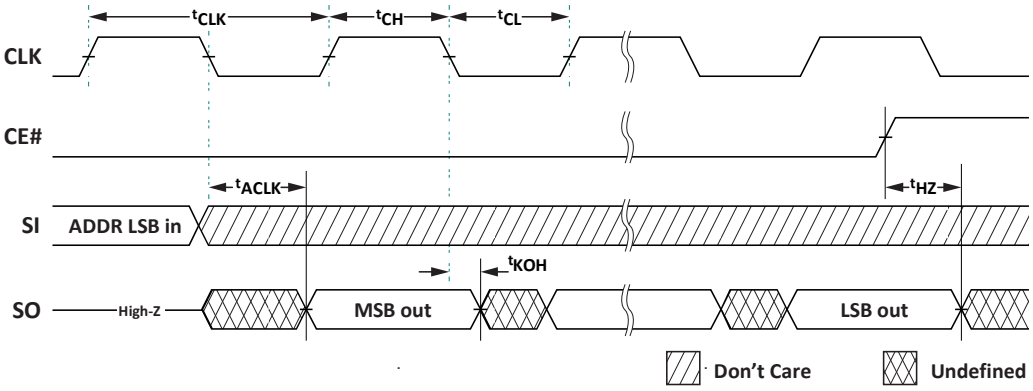


Figure 26: Output Timing

19 Electrical Specifications:

19.1 Absolute Maximum Ratings

Table 6: Absolute Maximum Ratings

Parameter	*Symbol*	*Rating*	*Unit*	*Notes*
Voltage to any ball except V_{DD} relative to V_{SS}	VT	-0.4 to V_{DD}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

19.2 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between VSS and VDD. During voltage transitions, inputs or I/Os may negative overshoot VSS to -1.0V or positive overshoot to VDD +1.0V, for periods up to 20 ns.

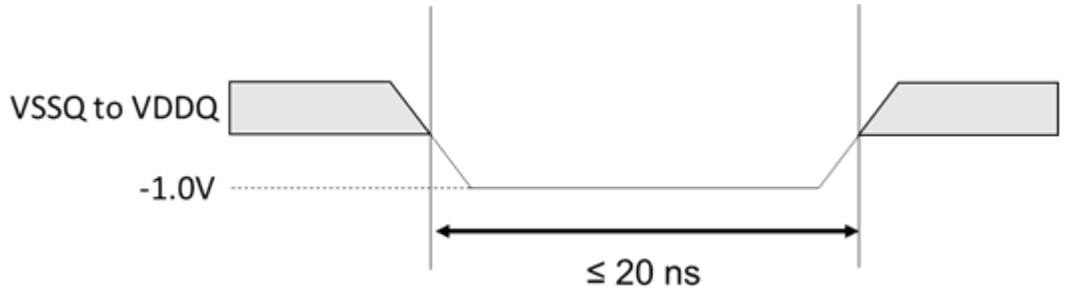


Figure 11 Maximum Negative Overshoot Waveform

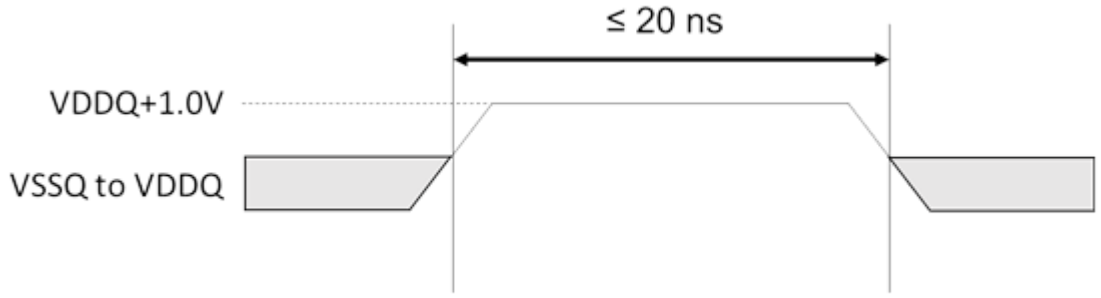


Figure 12 Maximum Positive Overshoot Waveform

19.3 Pin Capacitance

Table 7: Bare Die Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note: spec'd at 25°C.

Table 8: Package Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note: spec'd at 25°C.

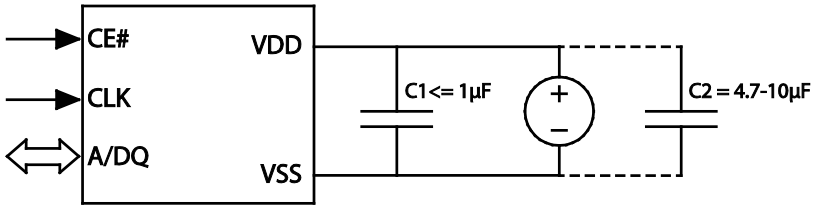
Table 9: Load Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

19.4 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



19.4.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

19.4.2 Large cap C2:

Though half-sleep average current is small (less than 100µA), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7µF-10µF cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

If needed, contact AP Memory for further decoupling solution assistance.

19.5 Operating Conditions

Table 10: Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

19.6 DC Characteristics

Table 11: DC Characteristics

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write (144MHz)		11	mA	1,2
	Read/Write (66MHz)		8.5	mA	1,2
	Read/Write (13MHz)		6	mA	1,2
ISB_{EXT}	Standby current (105C)		590	µA	3
ISB_{STD}	Standby current (85C)		420	µA	3

Note 1: Output load current not included.
2: 50% bus toggling rate.
3: Standby current is measured when CLK is in DC low state.
4: Typical ISBSTD 64µA.at 25°C
5: Typical ISB_{STD_HS} is 19.5µA.

19.7 AC Characteristics

Table 12: READ/WRITE Timing

Symbol	Parameter	Min	Max	Unit	Notes
^{t}CLK	CLK period - SPI Read (‘h03)	30.3		ns	33MHz
	CLK period - QPI Read (‘h0B)	15.1			66MHz
	CLK period - all other operations	7			144MHz*1,2,3
^{t}CH/^{t}CL	Clock high/low width	0.45	0.55	^{t}CLK(min)	
^{t}KHKL	CLK rise or fall time		1.1	ns	4
^{t}CPH	CE# HIGH between subsequent burst operations	18		ns	
^{t}CEM	CE# low pulse width (excluding Halfsleep™ Exit)		8	µs	Standard temp
			3		Extended temp
^{t}CSP	CE# setup time to CLK rising edge PKG	2.5		ns	2
^{t}CHD	CE# hold time from CLK rising edge PKG	3		ns	2
^{t}SP	Setup time to active CLK edge	2		ns	
^{t}HD	Hold time from active CLK edge	2		ns	
^{t}CHD_HS	CE# hold time from CLK rising edge for Halfsleep™ Entry command	6		ns	
^{t}HZ	Chip disable to DQ output high-Z		6	ns	
^{t}ACLK	CLK to output delay	2	5.5	ns	3
^{t}KOH	Data hold time from clock falling edge	1.5		ns	
^{t}HS	Minimum Halfsleep™ duration	150		µs	
^{t}XHS	Halfsleep™ Exit CE# low to CLK setup time	150		µs	
^{t}XPHS	Halfsleep™ Exit CE# low pulse width	60		ns	
			tCEM	µs	
^{t}RST	Time between end of RST CMD to next valid CMD	50		ns	

Note 1: Only Linear 2048 Burst allows page boundary crossing. Frequency limits are therefore 144MHz max for Wrapped Burst operation,
84MHz max when Linear 2048 Burst commands cross page boundary

2: System max C_L 15pF for the use of package.

3: For operating frequencies >84MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).

4: Measured from 20% to 80% of VDD

20 Change Log

Version	Who	Date	Description
0.1	Kim	Jun 17, 2022	Initial Version derived from E8 SQPI WLCSP
1.0	Kim	Nov 30, 2023	Modify Standby and Halfsleep typical current Add chapter 19.2 Input signal overshoot